Document Title

128M x 8 Bit / 64M x 16 Bit NAND Flash Memory

Revision History

Revision No	History	Draft Date	Remark
0.0	1. Initial issue	July. 5. 2001	Advance
0.1	1. Iol(R/B) of 1.8V is changed. - min. value : 7mA --> 3mA - Typ. value : 8mA --> 4mA	Nov. 5. 2001	
	2. AC parameter is changed. tRP(min.) : 30ns --> 25ns		
	3. A recovery time of minimum 1µs is required before internal circuit gets ready for any command sequences as shown in Figure 17. ---> A recovery time of minimum 10µs is required before internal circuit gets ready for any command sequences as shown in Figure 17.	Dec. 4. 2001	
0.2	1. ALE status fault in 'Random data out in a page' timing diagram(page 19) is fixed.		
0.3	1. tAR1, tAR2 are merged to tAR.(Page11) (Before revision) min. tAR1 = 10ns , min. tAR2 = 50ns (After revision) min. tAR = 10ns 2. min. tCLR is changed from 50ns to 10ns.(Page11) 3. min. tREA is changed from 35ns to 30ns.(Page11) 4. min. tWC is changed from 50ns to 45ns.(Page11) 5. tRHZ is devided into tRHZ and tOH.(Page11) - tRHZ : $\overline{RE}$ High to Output Hi-Z - tOH : $\overline{RE}$ High to Output Hold 6. tCHZ is devided into tCHZ and tOH.(Page11) - tCHZ : $\overline{CE}$ High to Output Hi-Z - tOH : $\overline{CE}$ High to Output Hold	Apr. 25. 2002	
0.4	1. Add the Rp vs tr ,tf & Rp vs ibusy graph for 1.8V device (Page 35) 2. Add the data protection Vcc guidence for 1.8V device - below about 1.1V. (Page 36)	Nov. 22.2002	
0.5	1. The min. Vcc value 1.8V devices is changed. K9F1GXXQ0M : Vcc 1.65V~1.95V --> 1.70V~1.95V	Mar. 6.2003	
0.6	Pb-free Package is added. K9F1G08U0M-FCB0,FIB0 K9F1G08Q0M-PCB0,PIB0 K9F1G08U0M-PCB0,PIB0 K9F1G16U0M-PCB0,PIB0 K9F1G16Q0M-PCB0,PIB0	Mar. 13.2003	

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Revision History

Revision No	History	Draft Date	Remark
0.7	Errata is added.(Front Page)-K9F1GXXQ0M tWC tWP tWH tRC tREH tRP tREA tCEA Specification 45 25 15 50 15 25 30 45 Relaxed value 80 60 20 80 20 60 60 75	Mar.17. 2003	
0.8	1. The 3rd Byte ID after 90h ID read command is don't cared. The 5th Byte ID after 90h ID read command is deleted.	Apr. 9. 2003	
0.9	1. 2.65V device is added. 2. Note is added. (VIL can undershoot to -0.4V and VIH can overshoot to VCC +0.4V for durations of 20 ns or less.)	Jul. 2. 2003	
1.0	AC parameters are changed-K9F1GXXQ0M tWC tWP tWH tRC tREH tRP tREA tCEA Before 45 25 15 50 15 25 30 45 After 80 60 20 80 20 60 60 75	Aug. 5. 2003	
1.1	Added Addressing method for program operation	Jan. 27. 2004	
1.2	1. Add the Protrusion/Burr value in WSOP1 PKG Diagram.	Apr. 23. 2004	
1.3	1. PKG(TSOP1, WSOP1) Dimension Change	May. 24. 2004	

128M x 8 Bit / 64M x 16 Bit NAND Flash Memory

PRODUCT LIST

Part Number	Vcc Range	Organization	PKG Type
K9F1G08Q0M-Y,P	1.70 ~ 1.95V	X8	TSOP1
K9F1G16Q0M-Y,P		X16	
K9F1G08D0M-Y,P	2.4 ~ 2.9V	X8	TSOP1
K9F1G16D0M-Y,P		X16	
K9F1G08U0M-Y,P	2.7 ~ 3.6V	X8	TSOP1
K9F1G16U0M-Y,P		X16	
K9F1G08U0M-V,F		X8	WSOP1

FEATURES

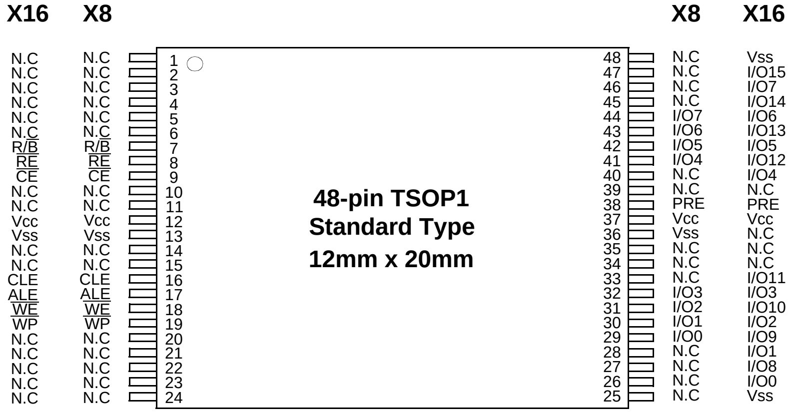
- Voltage Supply
  - -1.8V device(K9F1GXXQ0M): 1.70V~1.95V
  - - 2.65V device(K9F1GXXD0M) : 2.4~2.9V
  - -3.3V device(K9F1GXXU0M): 2.7 V ~3.6 V
- Organization
  - Memory Cell Array
    - -X8 device(K9F1G08X0M) : (128M + 4,096K)bit x 8bit
    - -X16 device(K9F1G16X0M) : (64M + 2,048K)bit x 16bit
  - Data Register
    - -X8 device(K9F1G08X0M): (2K + 64)bit x8bit
    - -X16 device(K9F1G16X0M): (1K + 32)bit x16bit
  - Cache Register
    - -X8 device(K9F1G08X0M): (2K + 64)bit x8bit
    - -X16 device(K9F1G16X0M): (1K + 32)bit x16bit
- Automatic Program and Erase
  - Page Program
    - -X8 device(K9F1G08X0M): (2K + 64)Byte
    - -X16 device(K9F1G16X0M): (1K + 32)Word
  - Block Erase
    - -X8 device(K9F1G08X0M): (128K + 4K)Byte
    - -X16 device(K9F1G16X0M): (64K + 2K)Word
- Page Read Operation
  - Page Size
    - - X8 device(K9F1G08X0M): 2K-Byte
    - - X16 device(K9F1G16X0M) : 1K-Word
  - Random Read : 25µs(Max.)
  - Serial Access : 50ns(Min.)*
    *K9F1GXXQ0M : 80ns
- Fast Write Cycle Time
  - Program time : 300µs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Cache Program Operation for High Performance Program
- Power-On Auto-Read Operation
- Intelligent Copy-Back Operation
- Unique ID for Copyright Protection
- Package :
  - K9F1GXXX0M-YCB0/YIB0
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
  - K9F1G08U0M-VCB0/VIB0
    48 - Pin WSOP I (12X17X0.7mm)
  - K9F1GXXX0M-PCB0/PIB0
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)- Pb-free Package
  - K9F1G08U0M-FCB0/FIB0
    48 - Pin WSOP I (12X17X0.7mm)- Pb-free Package
    * K9F1G08U0M-V,F(WSOPI) is the same device as K9F1G08U0M-Y,P(TSOP1) except package type.

GENERAL DESCRIPTION

Offered in 128Mx8bit or 64Mx16bit, the K9F1GXXX0M is 1G bit with spare 32M bit capacity. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 300µs on the 2112-byte(X8 device) or 1056-word(X16 device) page and an erase operation can be performed in typical 2ms on a 128K-byte(X8 device) or 64K-word(X16 device) block. Data in the data page can be read out at 50ns(1.8V device : 80ns) cycle time per byte(X8 device) or word(X16 device).. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9F1GXXX0M′s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9F1GXXX0M is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

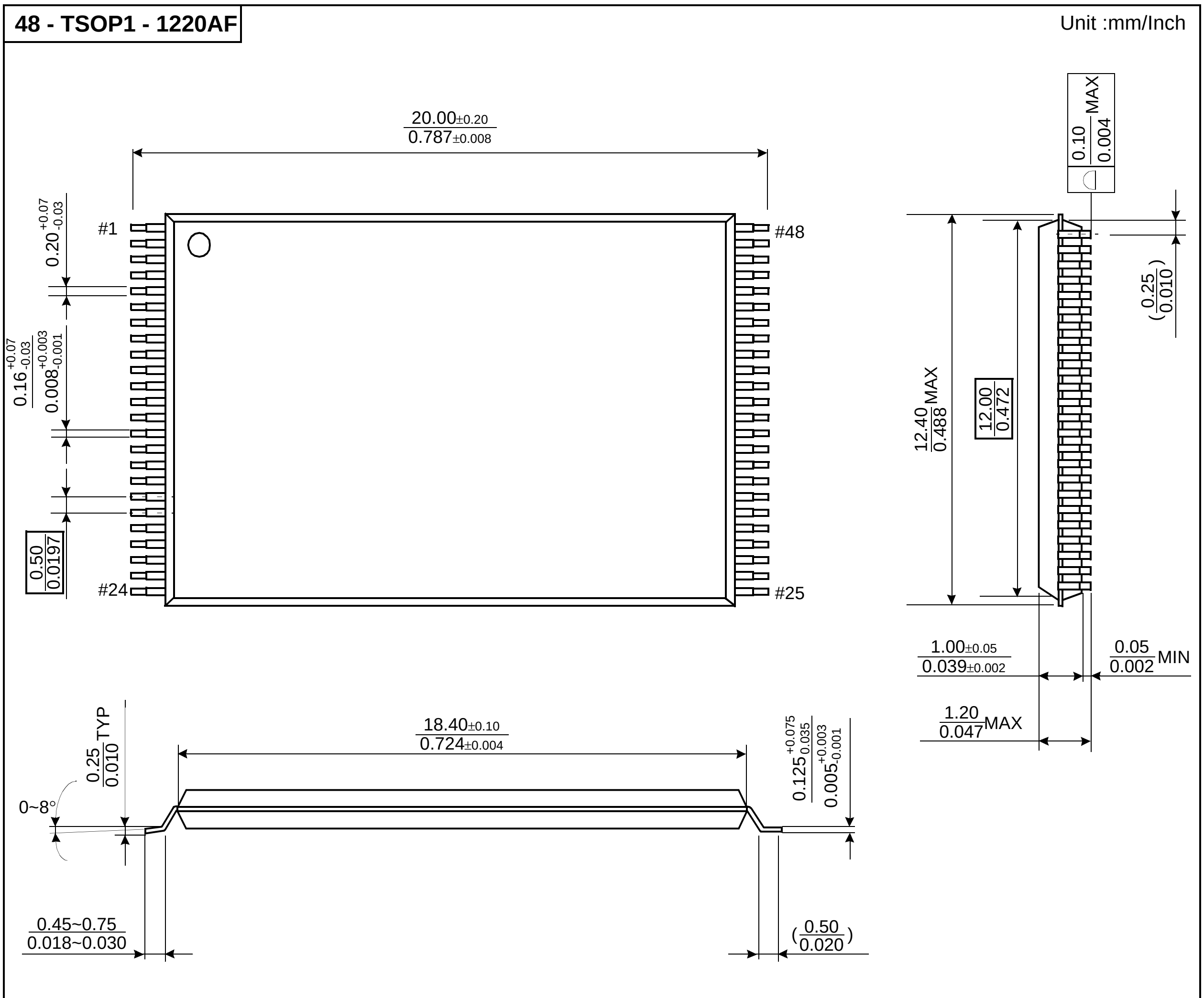
PIN CONFIGURATION (TSOP1)

K9F1GXXX0M-YCB0,PCB0/YIB0,PIB0



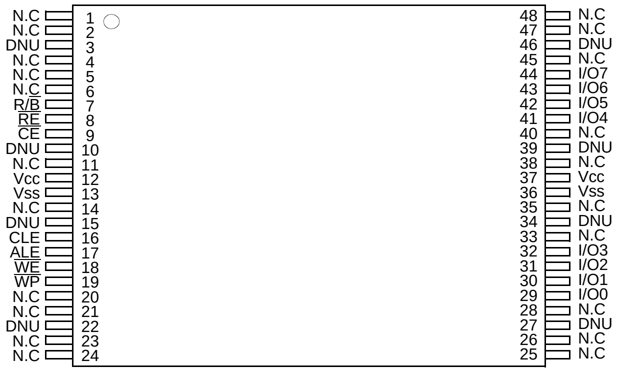
PACKAGE DIMENSIONS

48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)



PIN CONFIGURATION (WSOP1)

K9F1G08U0M-VCB0,FCB0/VIB0,FIB0

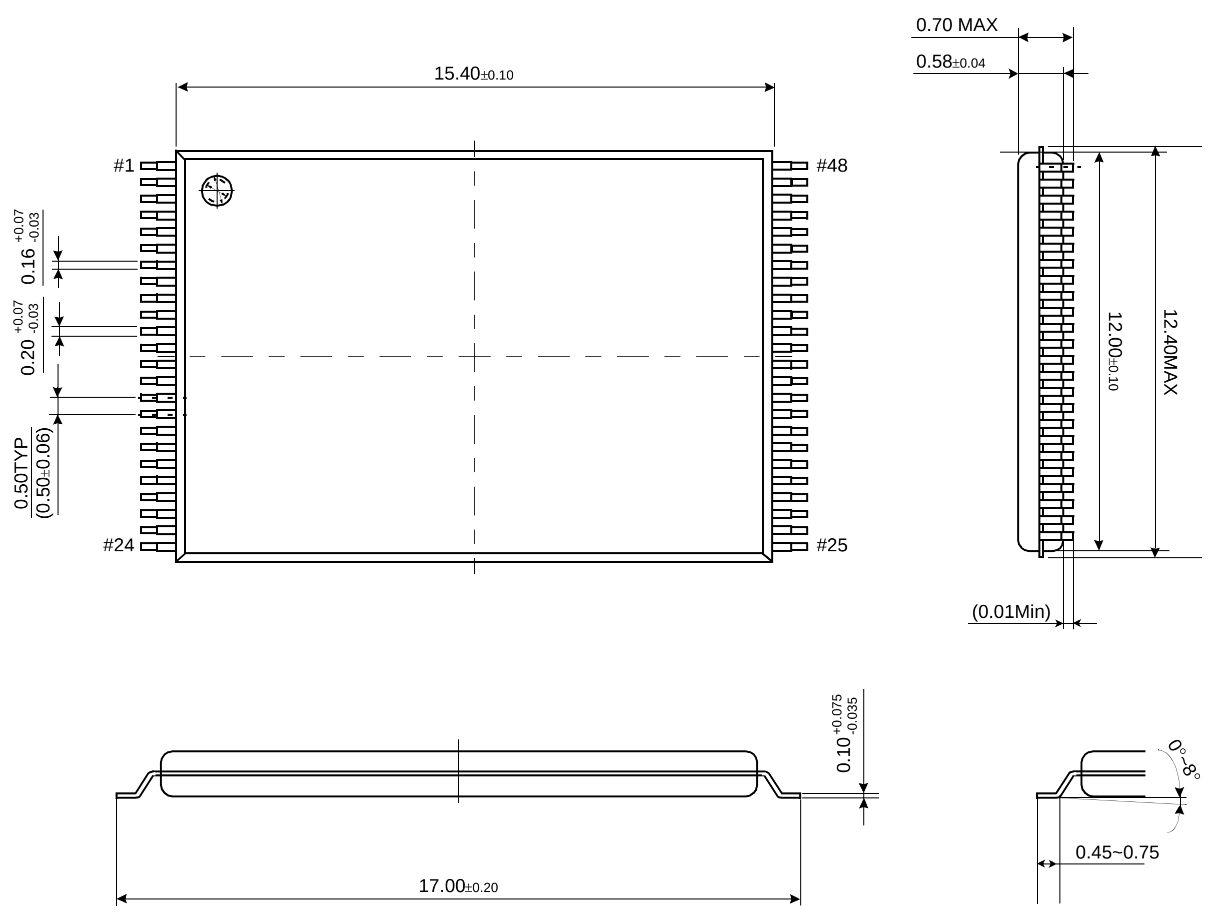


PACKAGE DIMENSIONS

48-PIN LEAD PLASTIC VERY VERY THIN SMALL OUT-LINE PACKAGE TYPE (I)

48 - WSOP1 - 1217F

Unit :mm



PIN DESCRIPTION

Pin Name	Pin Function
$I/O_0 \sim I/O_7$ (K9F1G08X0M) $I/O_0 \sim I/O_{15}$ (K9F1G16X0M)	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled. I/O8 ~ I/O15 are used only in X16 organization device. Since command input and address input are x8 operation, I/O8 ~ I/O15 are not used to input command & address. I/O8 ~ I/O15 are used only for data input and output.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
PRE	**POWER-ON READ ENABLE** The PRE controls auto read operation executed during power-on. The power-on auto-read is enabled when PRE pin is tied to Vcc.
Vcc	**POWER** VCC is the power supply for device.
Vss	**GROUND**
N.C	**NO CONNECTION** Lead is not internally connected.

NOTE : Connect all VCC and VSS pins of each device to common power supply outputs.
Do not leave VCC or VSS disconnected.

Figure 1-1. K9F1G08X0M (X8) Functional Block Diagram

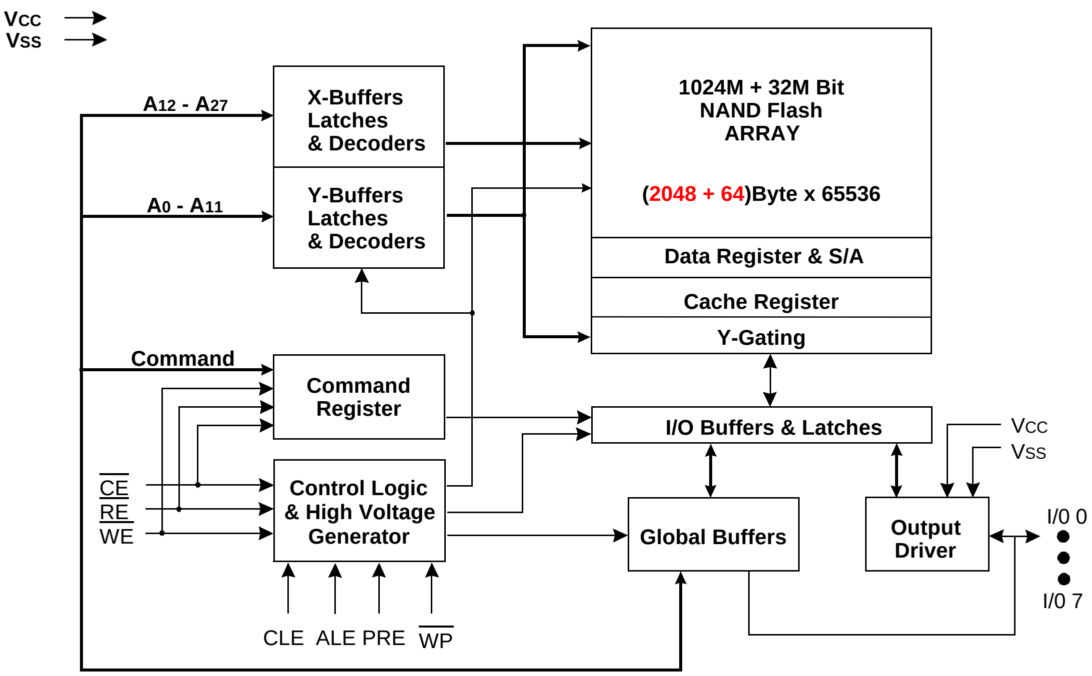
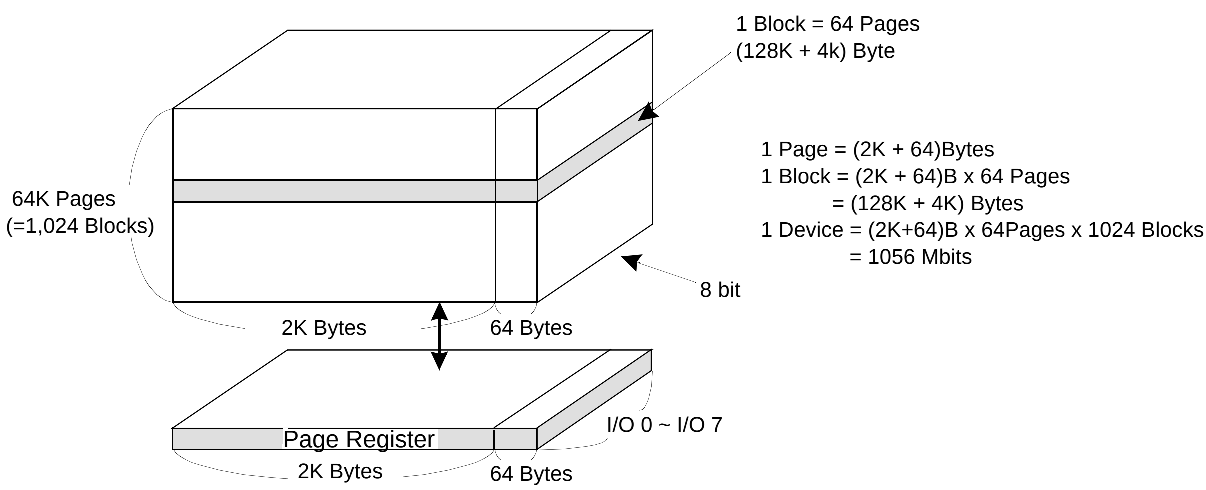


Figure 2-1. K9F1G08X0M (X8) Array Organization



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	**Column Address**
2nd Cycle	A_8	A_9	A_{10}	A_{11}	*L	*L	*L	*L	**Column Address**
3rd Cycle	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	**Row Address**
4th Cycle	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	**Row Address**

NOTE : Column Address : Starting Address of the Register.
* L must be set to "Low".
* The device ignores any additional input of address cycles than reguired.

Figure 1-2. K9F1G16X0M (X16) Functional Block Diagram

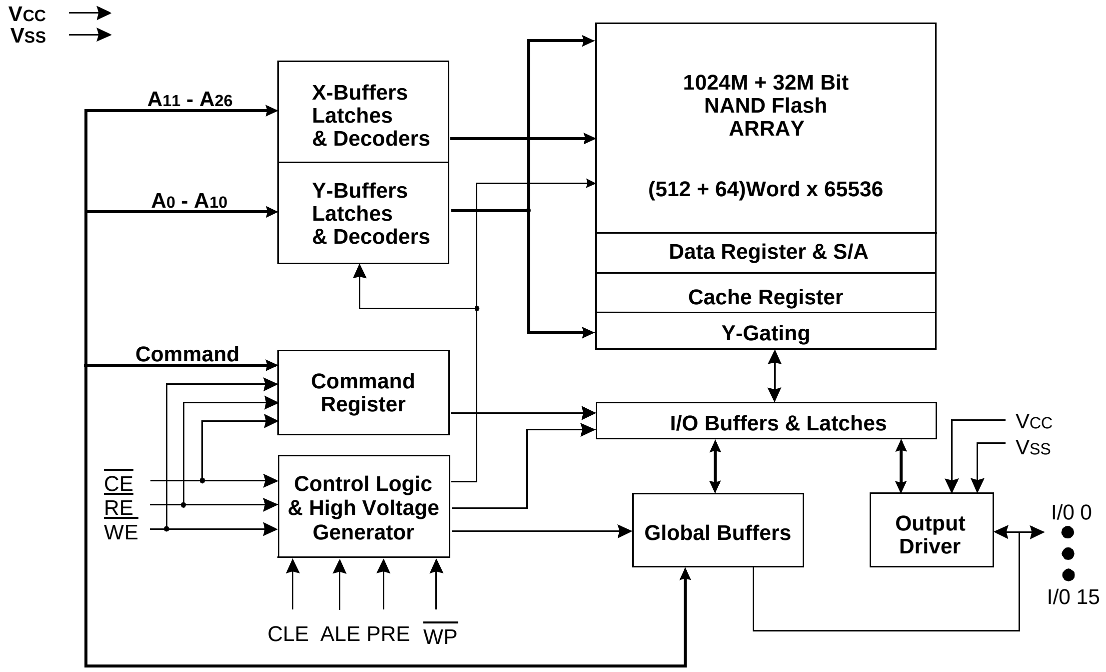
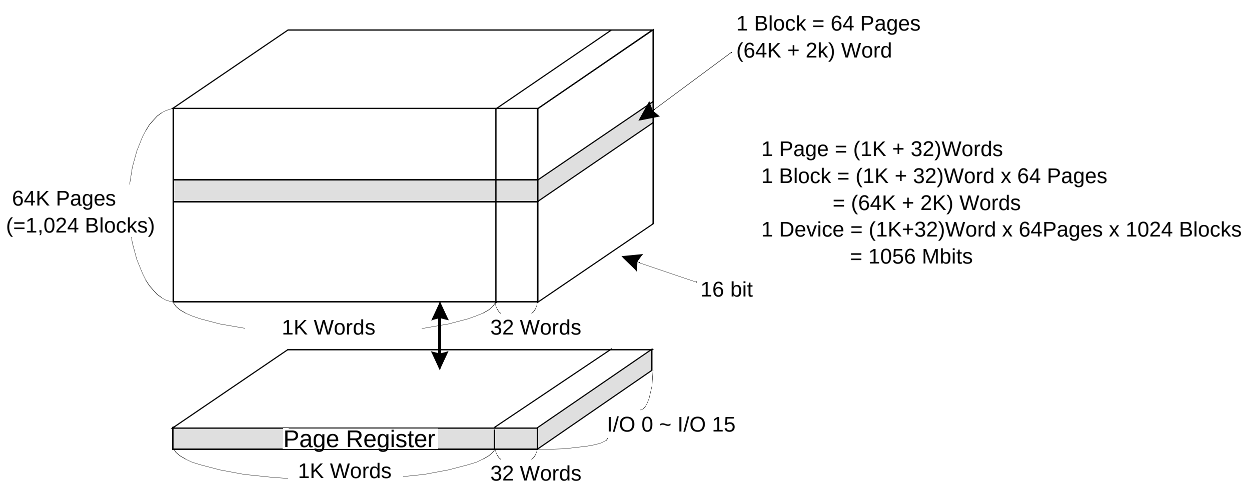


Figure 2-2. K9F1G16X0M (X16) Array Organization



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	I/O8 ~ 15	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	*L	**Column Address**
2nd Cycle	A_8	A_9	A_{10}	*L	*L	*L	*L	*L	*L	**Column Address**
3rd Cycle	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	*L	**Row Address**
4th Cycle	A_{19}	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	*L	**Row Address**

NOTE : Column Address : Starting Address of the Register.
* L must be set to "Low".
* The device ignores any additional input of address cycles than reguired.

Product Introduction

The K9F1GXXX0M is a 1056Mbit(1,107,296,256 bit) memory organized as 65,536 rows(pages) by 2112x8(X8 device) or 1056x16(X16 device) columns. Spare 64(X8) or 32(X16) columns are located from column address of 2048~2111(X8 device) or 1024~1055(X16 device). A 2112-byte(X8 device) or 1056-word(X16 device) data register and a 2112-byte(X8 device) or 1056-word(X16 device) cache register are serially connected to each other. Those serially connected registers are connected to memory cell arrays for accommodating data transfer between the I/O buffers and memory cells during page read and page program operations. The memory array is made up of 32 cells that are serially connected to form a NAND structure. Each of the 32 cells resides in a different page. A block consists of two NAND structured strings. A NAND structure consists of 32 cells. Total 1081344 NAND cells reside in a block. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 1024 separately erasable 128K-byte(X8 device) or 64K-word(X16 device) blocks. It indicates that the bit by bit erase operation is prohibited on the K9F1GXXX0M.

The K9F1GXXX0M has addresses multiplexed into 8 I/Os(X16 device case : lower 8 I/Os). This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE to low while CE is low. Those are latched on the rising edge of WE. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. The 128M byte(X8 device) or 64M word(X16 device) physical space requires 28(X8) or 27(X16) addresses, thereby requiring four cycles for addressing: 2 cycles of column address, 2 cycles of row address, in that order. Page Read and Page Program need the same four address cycles following the required command input. In Block Erase operation, however, only the two row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9F1GXXX0M.

The device provides cache program in a block. It is possible to write data into the cache registers while data stored in data registers are being programmed into memory cells in cache program mode. The program performace may be dramatically improved by cache program when there are lots of pages of data to be programmed.

The device embodies power-on auto-read feature which enables serial access of data of the 1st page without command and address input after power-on.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory. Since the time-consuming serial access and data-input cycles are removed, system performance for solid-state disk application is significantly increased.

Table 1. Command Sets

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Cache Program	80h	15h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input*	85h	-	
Random Data Output*	05h	E0h	
Read Status	70h		O

NOTE : 1. Random Data Input/Output can be executed in a page.
2. Command not specified in command sets table is not permitted to be entered to the device, which can raise erroneous operation.

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			1.8V DEVICE	3.3V/2.65V DEVICE	
Voltage on any pin relative to VSS		VIN/OUT	-0.6 to + 2.45	-0.6 to + 4.6	V
		VCC	-0.2 to + 2.45	-0.6 to + 4.6	
Temperature Under Bias	K9F1GXXX0M-XCB0	TBIAS	-10 to +125		°C
	K9F1GXXX0M-XIB0		-40 to +125		
Storage Temperature	K9F1GXXX0M-XCB0	TSTG	-65 to +150		°C
	K9F1GXXX0M-XIB0				
Short Circuit Current		Ios	5		mA

NOTE :
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is VCC,+0.3V which, during transitions, may overshoot to VCC+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, K9F1GXXX0M-XCB0 :TA=0 to 70°C, K9F1GXXX0M-XIB0:TA=-40 to 85°C)

Parameter	Symbol	K9F1GXXQ0M(1.8V)			K9F1GXXD0M(2.65V)			K9F1GXXU0M(3.3V)			Unit
		Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max	
Supply Voltage	VCC	1.70	1.8	1.95	2.4	2.65	2.9	2.7	3.3	3.6	V
Supply Voltage	VSS	0	0	0	0	0	0	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	K9F1GXXX0M									Unit
				1.8V			2.65V			3.3V			
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Operating Current	Page Read with Serial Access	$I_{CC}1$	tRC=50ns, $\overline{CE}=V_{IL}$ I_{OUT}=0mA	-	8	15	-	10	20	-	10	20	mA
	Program	$I_{CC}2$	-	-	8	15	-	10	20	-	10	20	
	Erase	$I_{CC}3$	-	-	8	15	-	10	20	-	10	20	
Stand-by Current(TTL)		$I_{SB}1$	$\overline{CE}=V_{IH}$, $\overline{WP}=\overline{PRE}$=0V/$V_{CC}$	-	-	1	-	-	1	-	-	1	
Stand-by Current(CMOS)		$I_{SB}2$	$\overline{CE}=V_{CC}$-0.2, $\overline{WP}=\overline{PRE}$=0V/$V_{CC}$	-	10	50	-	10	50	-	10	50	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±10	-	-	±10	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10	-	-	±10	-	-	±10	
Input High Voltage		V_{IH}*	-	V_{CC} -0.4	-	V_{CC} +0.3	V_{CC} -0.4	-	V_{CC} +0.3	2.0	-	V_{CC} +0.3	V
Input Low Voltage, All inputs		V_{IL}*	-	-0.3	-	0.4	-0.3	-	0.5	-0.3	-	0.8	
Output High Voltage Level		V_{OH}	K9F1GXXQ0M :I_{OH}=-100µA K9F1GXXD0M :I_{OH}=-100µA K9F1GXXU0M :I_{OH}=-400µA	Vcc -0.1	-	-	V_{CCQ} -0.4	-	-	2.4	-	-	
Output Low Voltage Level		V_{OL}	K9F1GXXQ0M :I_{OL}=100uA K9F1GXXD0M :I_{OL}=100µA K9F1GXXU0M :I_{OL}=2.1mA	-	-	0.1	-	-	0.4	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	K9F1GXXQ0M :V_{OL}=0.1V K9F1GXXD0M :V_{OL}=0.1V K9F1GXXU0M :V_{OL}=0.4V	3	4	-	3	4	-	8	10	-	mA

NOTE : V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC} +0.4V for durations of 20 ns or less.

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	1004	-	1024	Blocks

NOTE :
1. The K9F1GXXX0M may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block, does not require Error Correction up to 1K program/erase cycles.

AC TEST CONDITION

(K9F1GXXX0M-XCB0 :TA=0 to 70°C, K9F1GXXX0M-XIB0:TA=-40 to 85°C

K9F1GXXQ0M : Vcc=1.70V~1.95V, K9F1GXXD0M : Vcc=2.4V~2.9V , K9F1GXXU0M : Vcc=2.7V~3.6V unless otherwise noted)

Parameter	K9F1GXXQ0M	K9F1GXXD0M	K9F1GXXU0M
Input Pulse Levels	0V to Vcc	0V to Vcc	0.4V to 2.4V
Input Rise and Fall Times	5ns	5ns	5ns
Input and Output Timing Levels	Vcc/2	Vcc/2	1.5V
K9F1GXXQ0M:Output Load (Vcc:1.8V +/-10%) K9F1GXXD0M:Output Load (V_{CCQ}:2.65V +/-10%) K9F1GXXU0M:Output Load (Vcc:3.0V +/-10%)	1 TTL GATE and CL=30pF	1 TTL GATE and CL=30pF	1 TTL GATE and CL=50pF
K9F1GXXU0M:Output Load (Vcc:3.3V +/-10%)	-	-	1 TTL GATE and CL=100pF

CAPACITANCE(T_A=25°C, V_{CC}=1.8V/2.65V/3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	PRE	Mode	
H	L	L	↑	H	X	X	Read Mode	Command Input
L	H	L	↑	H	X	X		Address Input(4clock)
H	L	L	↑	H	H	X	Write Mode	Command Input
L	H	L	↑	H	H	X		Address Input(4clock)
L	L	L	↑	H	H	X	Data Input	
L	L	L	H	↓	X	X	Data Output	
X	X	X	X	H	X	X	During Read(Busy)	
X	X	X	X	X	H	X	During Program(Busy)	
X	X	X	X	X	H	X	During Erase(Busy)	
X	X(1)	X	X	X	L	X	Write Protect	
X	X	H	X	X	0V/Vcc(2)	0V/Vcc(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ and PRE should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		tPROG	-	300	700	µs
Dummy Busy Time for Cache Program		tCBSY		3	700	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	4	cycles
	Spare Array		-	-	4	cycles
Block Erase Time		tBERS	-	2	3	ms

NOTE : 1. Max. time of tCBSY depends on timing between internal program completion and data in

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min			Max			Unit
		K9F1GXXQ0M	K9F1GXXD0M	K9F1GXXU0M	K9F1GXXQ0M	K9F1GXXD0M	K9F1GXXU0M	
CLE setup Time	tCLS	0	0	0	-	-	-	ns
CLE Hold Time	tCLH	10	10	10	-	-	-	ns
$\overline{CE}$ setup Time	tCS	0	0	0	-	-	-	ns
$\overline{CE}$ Hold Time	tCH	10	10	10	-	-	-	ns
$\overline{WE}$ Pulse Width	tWP	60	25(1)	25(1)	-	-	-	ns
ALE setup Time	tALS	0	0	0	-	-	-	ns
ALE Hold Time	tALH	10	10	10	-	-	-	ns
Data setup Time	tDS	20	20	20	-	-	-	ns
Data Hold Time	tDH	10	10	10	-	-	-	ns
Write Cycle Time	tWC	80	45	45	-	-	-	ns
$\overline{WE}$ High Hold Time	tWH	20	15	15	-	-	-	ns

NOTE : 1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

AC Characteristics for Operation

Parameter	Symbol	Min			Max			Unit
		K9F1GXXQ0M	K9F1GXXD0M	K9F1GXXU0M	K9F1GXXQ0M	K9F1GXXD0M	K9F1GXXU0M	
Data Transfer from Cell to Register	tR	-	-	-	25	25	25	µs
ALE to $\overline{RE}$ Delay	tAR	10	10	10	-	-	-	ns
CLE to $\overline{RE}$ Delay	tCLR	10	10	10	-	-	-	ns
Ready to $\overline{RE}$ Low	tRR	20	20	20	-	-	-	ns
RE Pulse Width	tRP	60	25	25	-	-	-	ns
WE High to Busy	tWB	-	-	-	100	100	100	ns
Read Cycle Time	tRC	80	50	50	-	-	-	ns
$\overline{RE}$ Access Time	tREA	-	-	-	60	30	30	ns
$\overline{CE}$ Access Time	tCEA	-	-	-	75	45	45	ns
$\overline{RE}$ High to Output Hi-Z	tRHZ	-	-	-	30	30	30	ns
$\overline{CE}$ High to Output Hi-Z	tCHZ	-	-	-	20	20	20	ns
$\overline{RE}$ or $\overline{CE}$ High to Output hold	tOH	15	15	15	-	-	-	ns
$\overline{RE}$ High Hold Time	tREH	20	15	15	-	-	-	ns
Output Hi-Z to $\overline{RE}$ Low	tIR	0	0	0	-	-	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	tWHR	60	60	60	-	-	-	ns
Device Resetting Time (Read/Program/Erase)	tRST	-	-	-	5/10/500(1)	5/10/500(1)	5/10/500(1)	µs

NOTE: 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.

NAND Flash Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. Devices with invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block, does not require Error Correction up to 1K program/erase cycles.

Identifying Invalid Block(s)

All device locations are erased(FFh for X8, FFFFh for X16) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 1st byte(X8 device) or 1st word(X16 device) in the spare area. Samsung makes sure that either the 1st or 2nd page of every invalid block has non-FFh(X8) or non-FFFFh(X16) data at the column address of 2048(X8 device) or 1024(X16 device). Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the original invalid block information is prohibited.

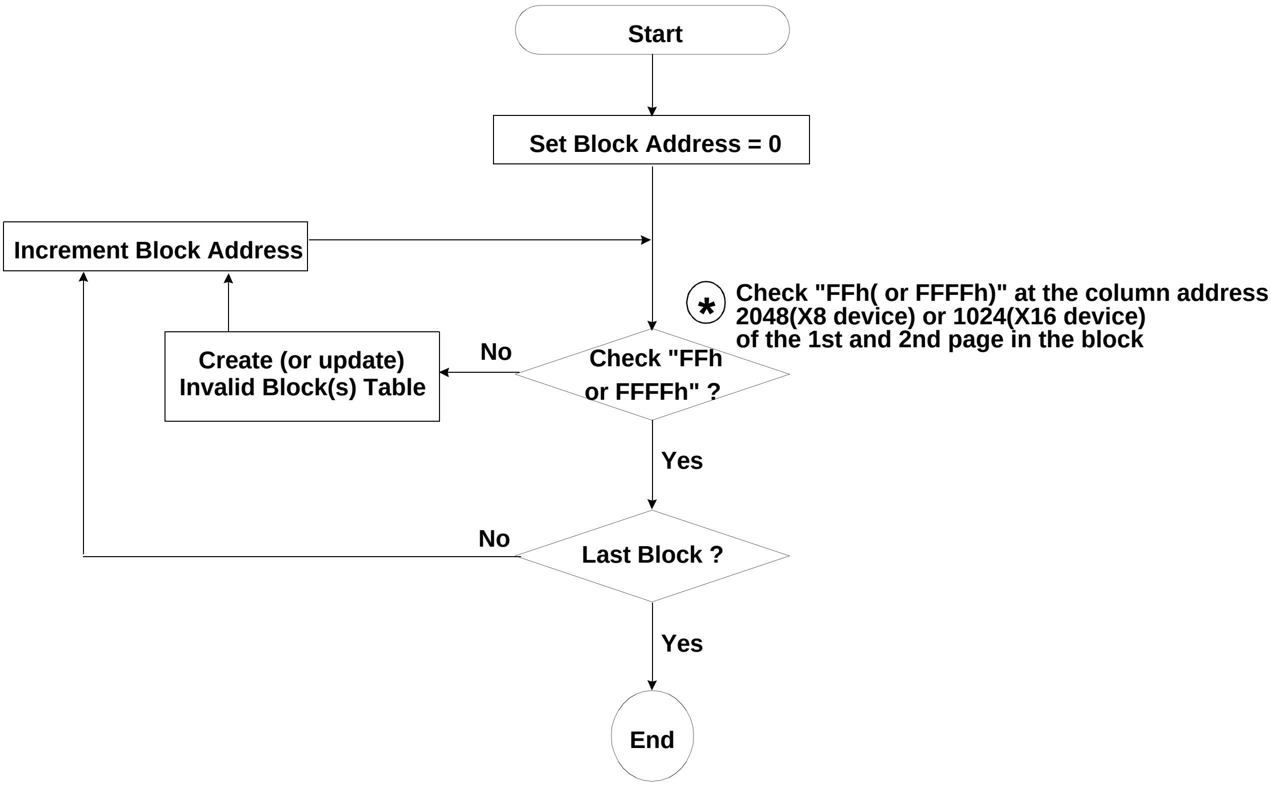


Figure 3. Flow chart to create invalid block table.

NAND Flash Technical Notes *(Continued)*

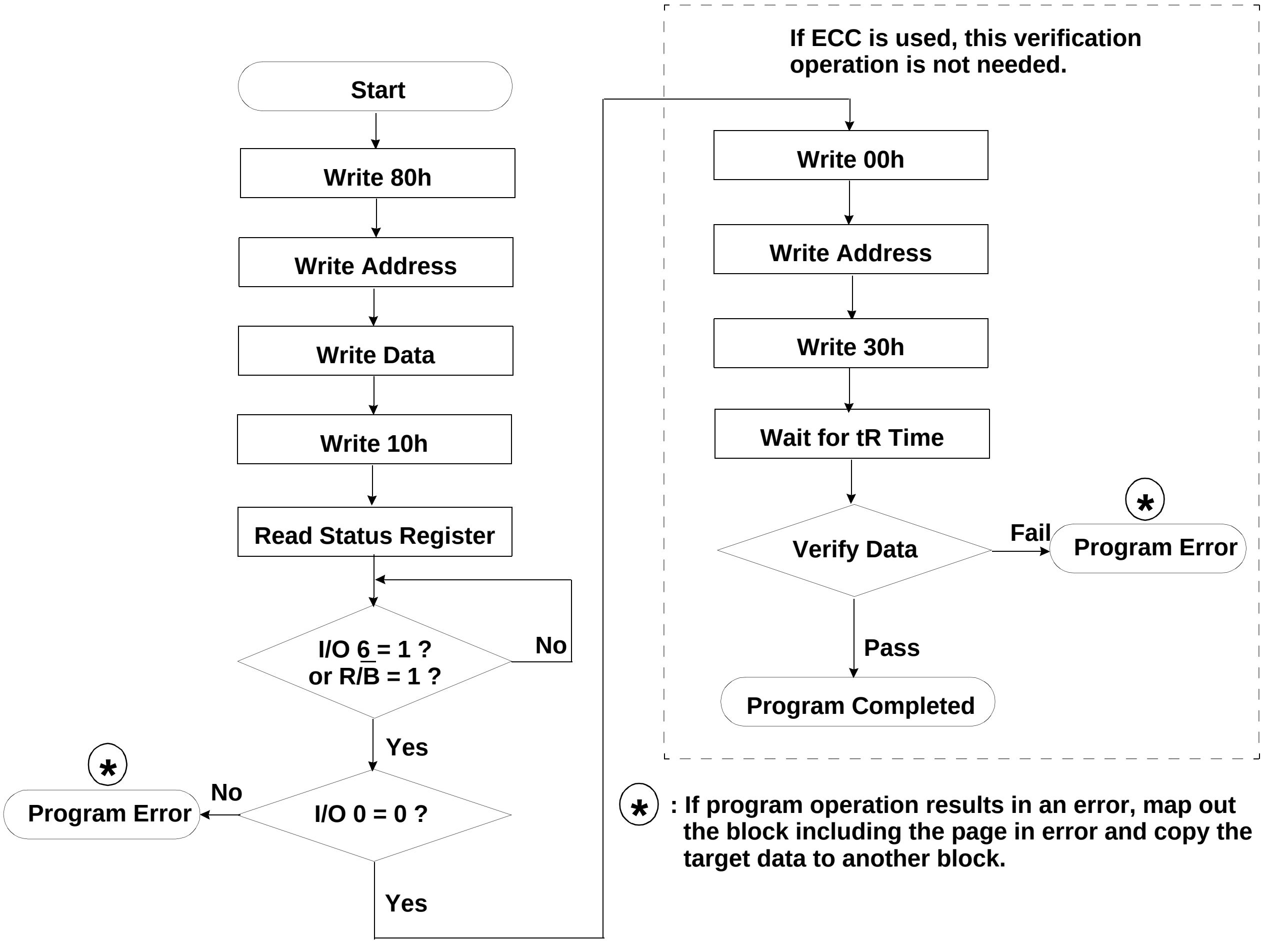
Error in write or read operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block.To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement or ECC Correction
Read	Single Bit Failure	Verify ECC -> ECC Correction

ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

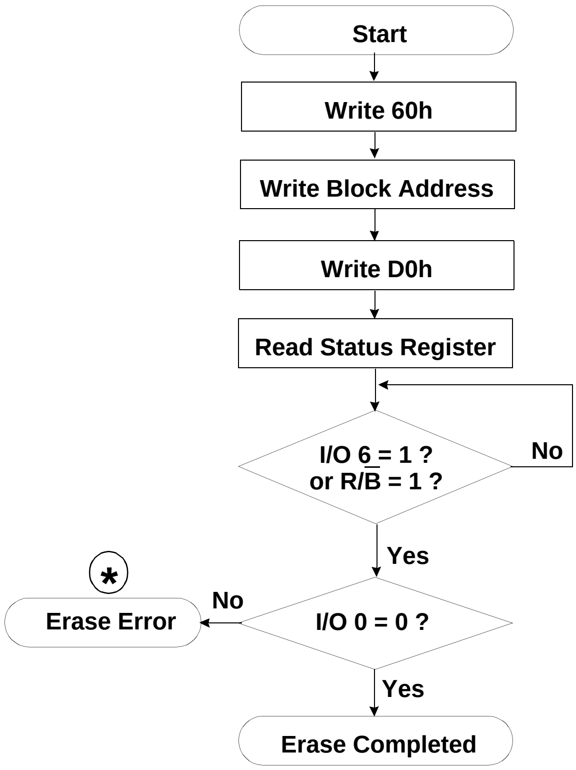
Program Flow Chart



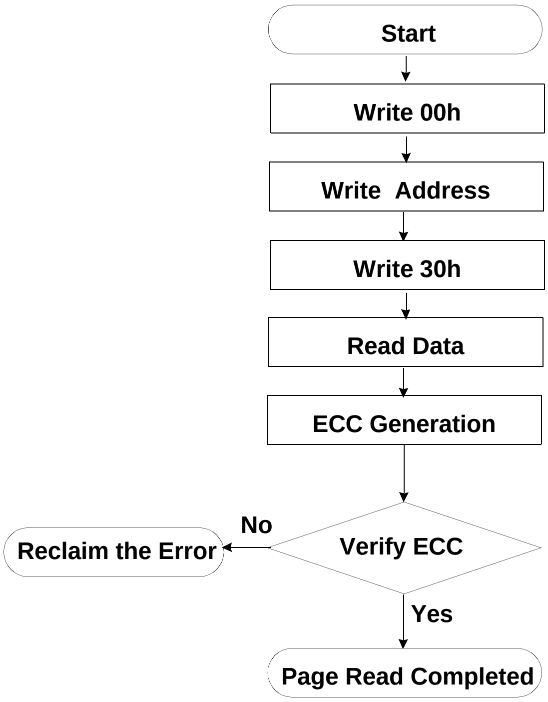
*: If program operation results in an error, map out the block including the page in error and copy the target data to another block.

NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

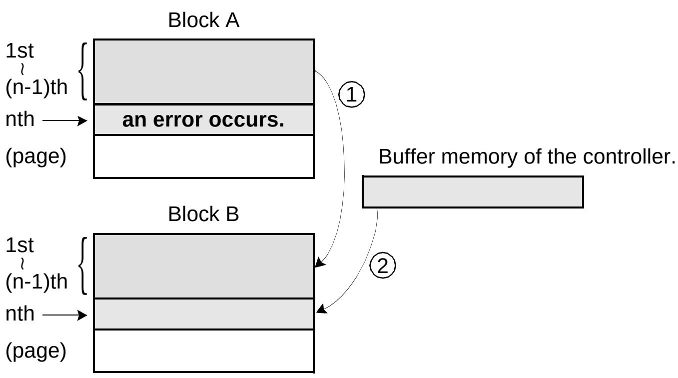


Read Flow Chart



*** : If erase operation results in an error, map out the failing block and replace it with another block.**

Block Replacement

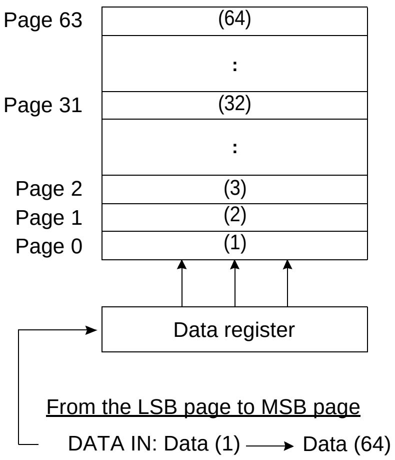


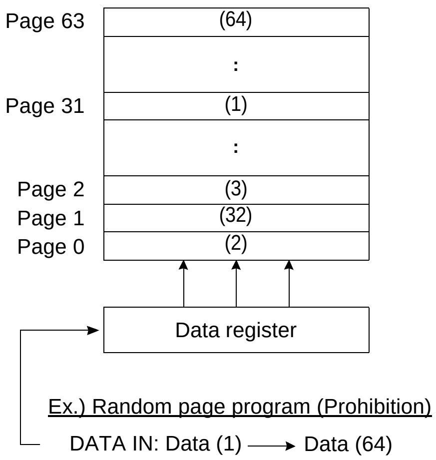
* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

NAND Flash Technical Notes *(Continued)*

Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited.





System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or serial access as shown below. The internal 2112byte(X8 device) or 1056word(X16 device) data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and serial access would provide significant savings in power consumption.

Figure 4. Program Operation with $\overline{CE}$ don't-care.

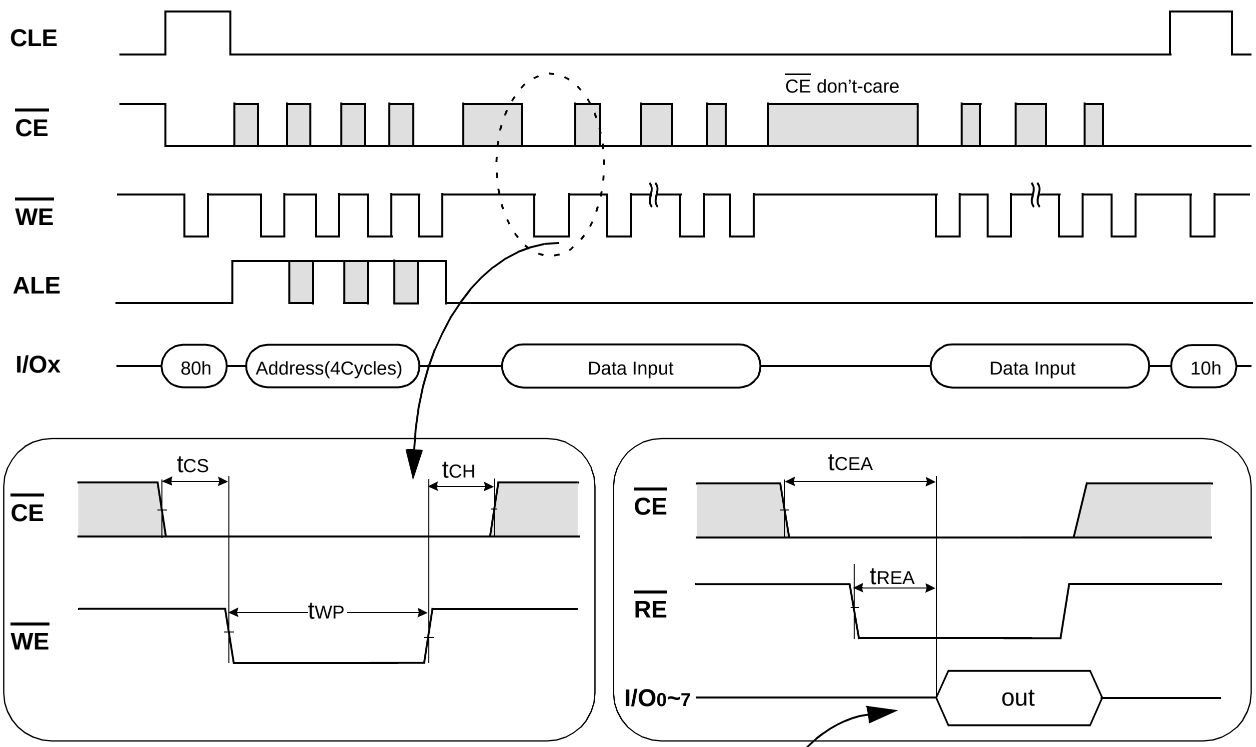
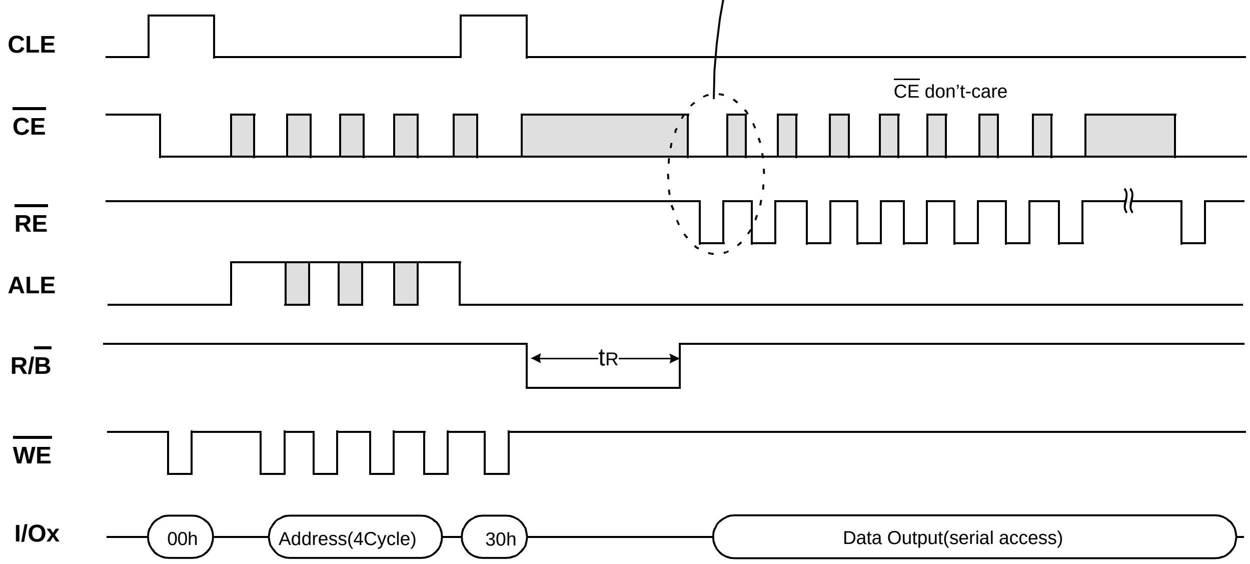


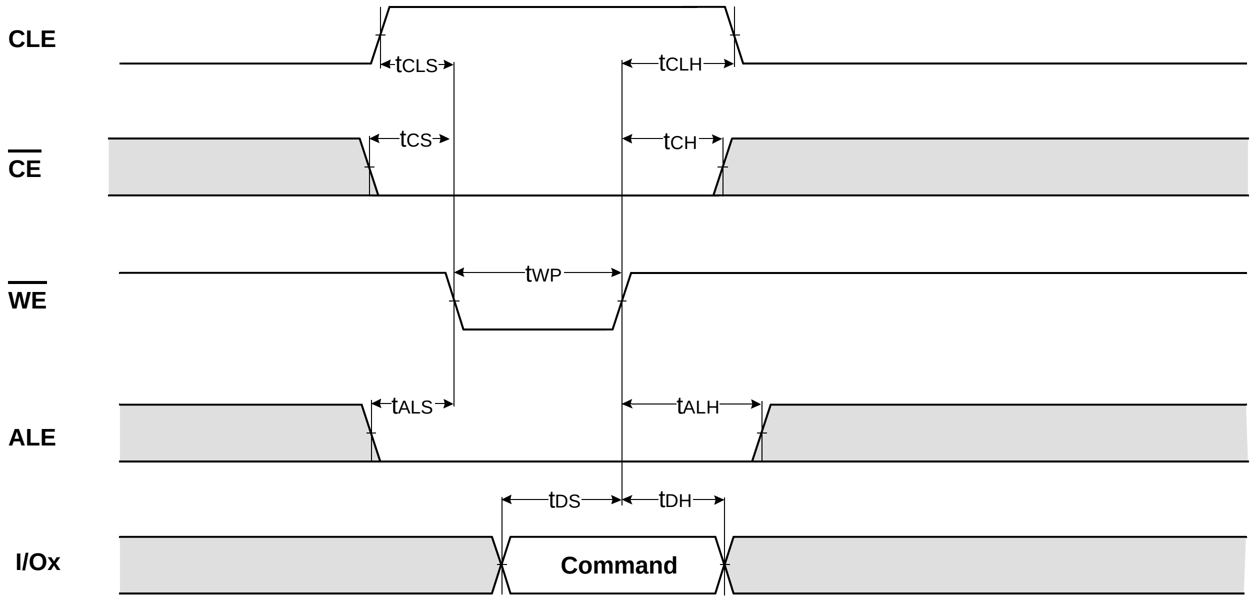
Figure 5. Read Operation with $\overline{CE}$ don't-care.



NOTE

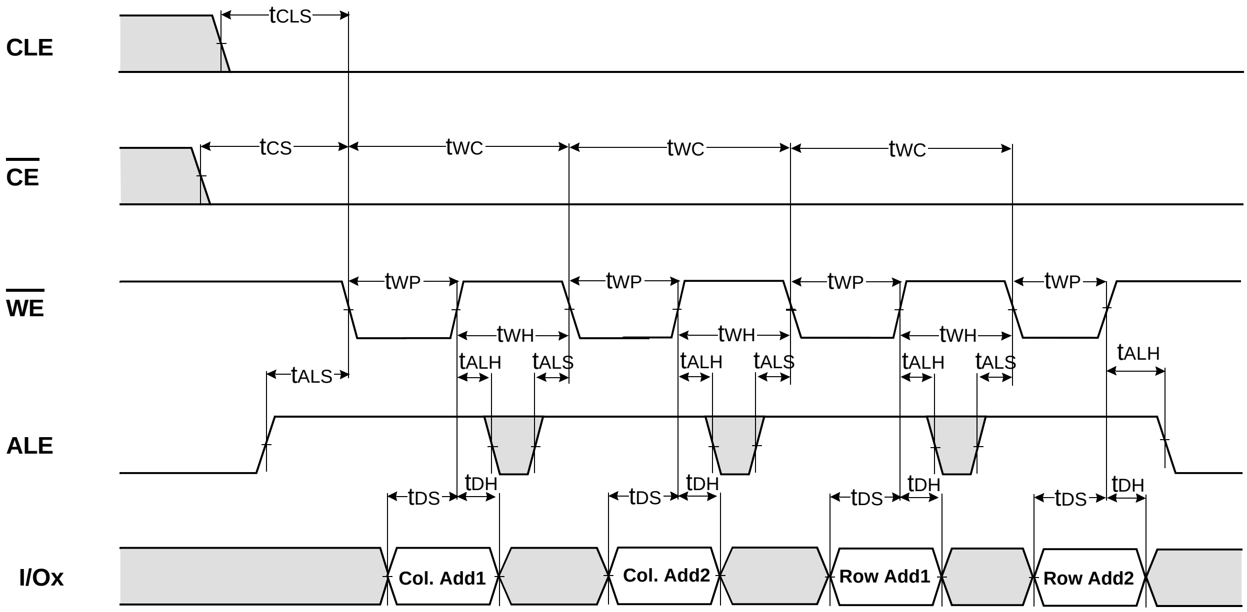
Device	I/O	DATA	ADDRESS			
	I/Ox	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2
K9F1G08X0M(X8 device)	I/O 0 ~ I/O 7	~2112byte	A0~A7	A8~A11	A12~A19	A20~A27
K9F1G16X0M(X16 device)	I/O 0 ~ I/O 15	~1056word	A0~A7	A8~A10	A11~A18	A19~A26

Command Latch Cycle



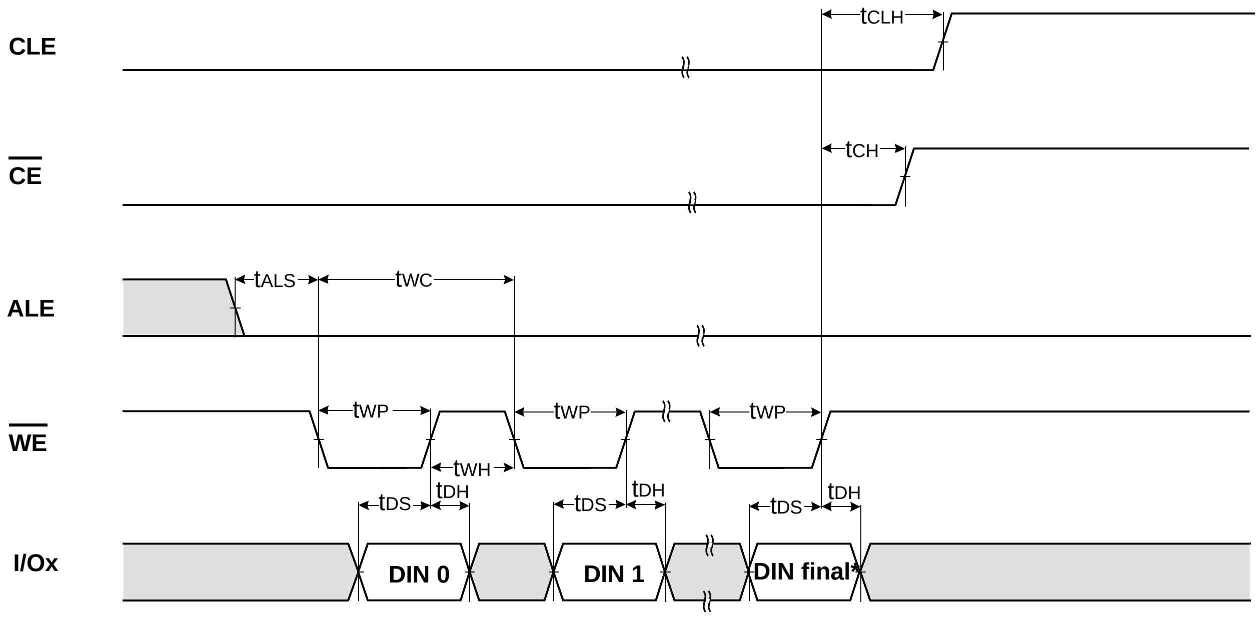
K9F1G16X0M : I/O8~15 must be set to "0"

Address Latch Cycle



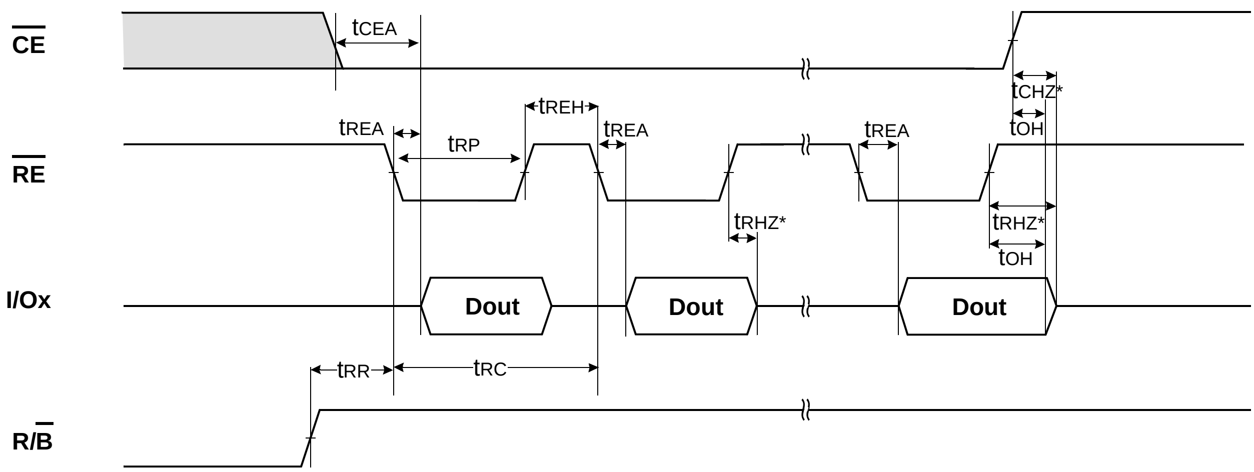
K9F1G16X0M : I/O8~15 must be set to "0"

Input Data Latch Cycle



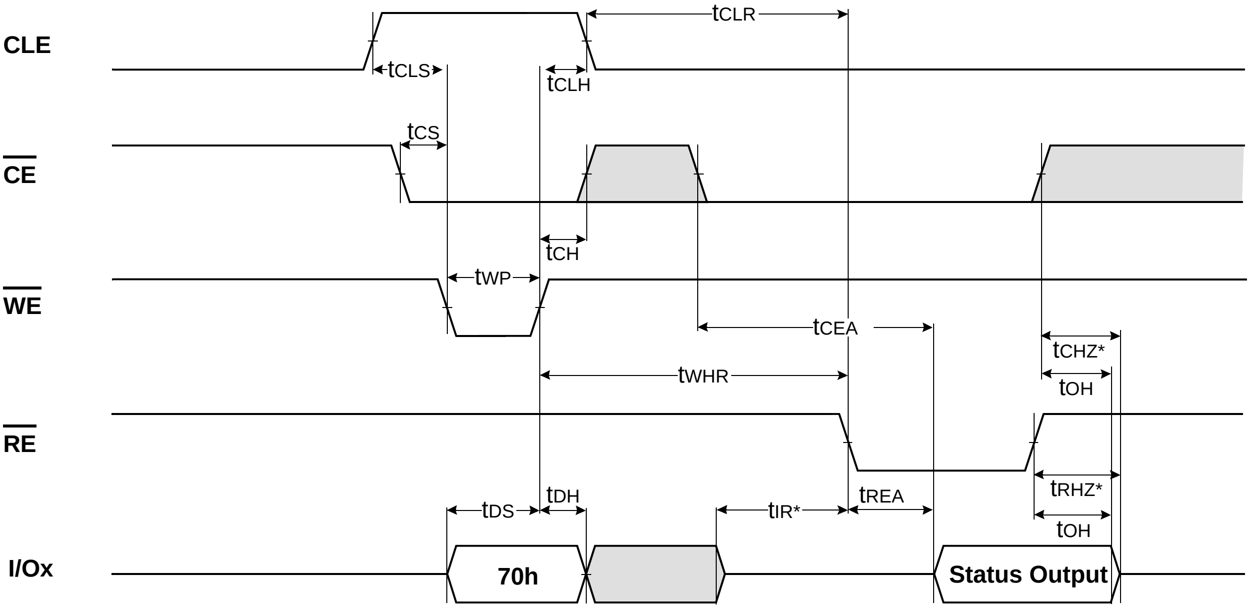
NOTES : DIN final means 2112(X8) or 1056(X16)

Serial Access Cycle after Read(CLE=L, WE=H, ALE=L)



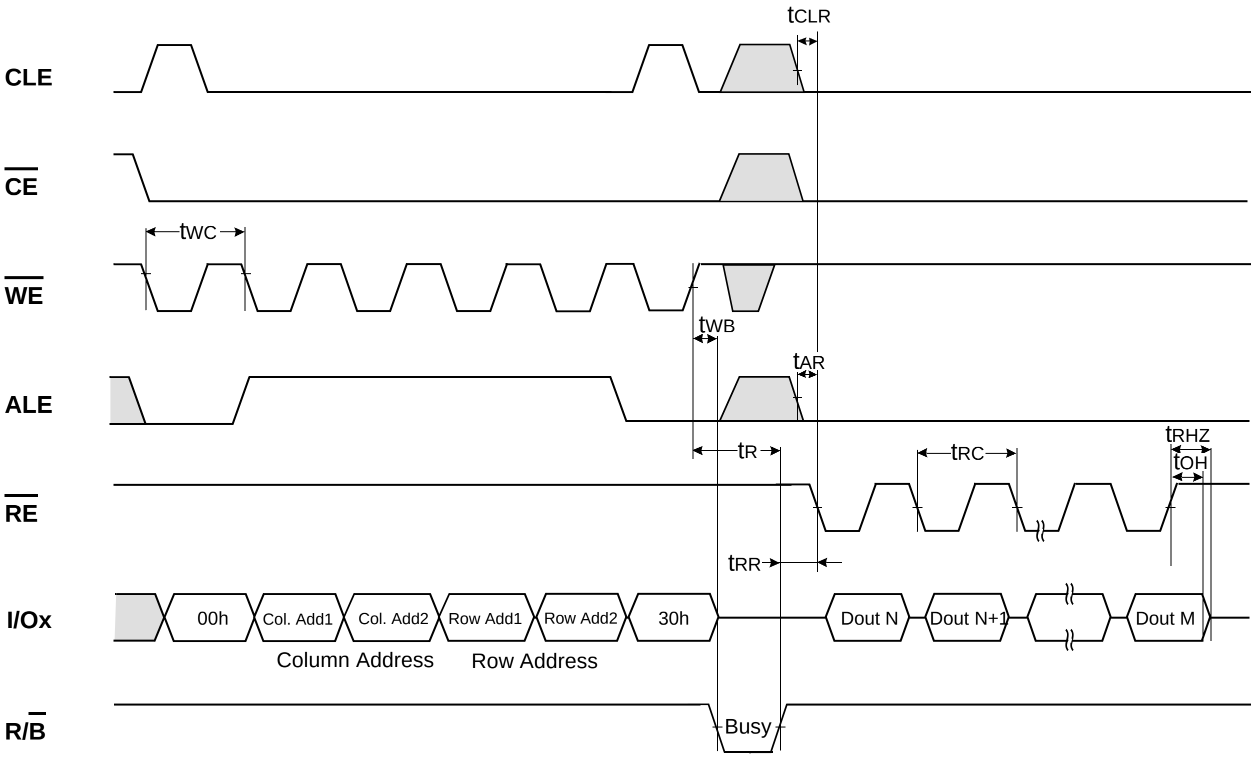
NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

Status Read Cycle

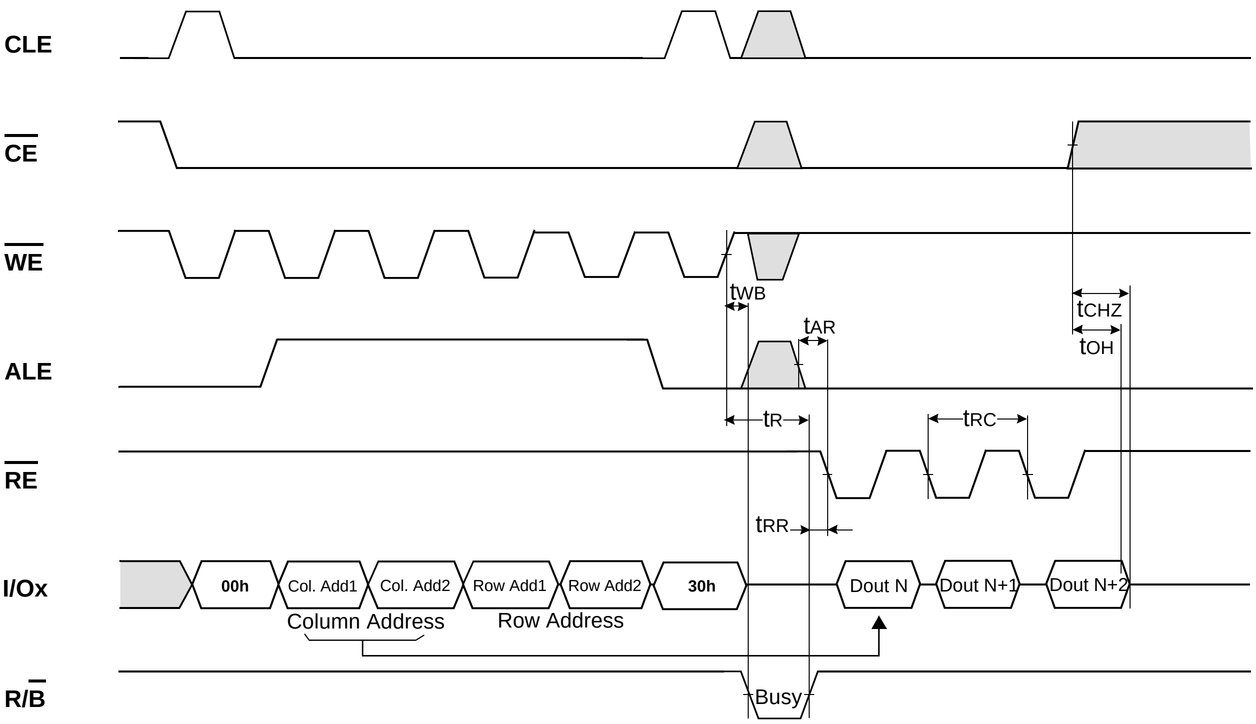


K9F1G16X0M : I/O8~15 must be set to "0"

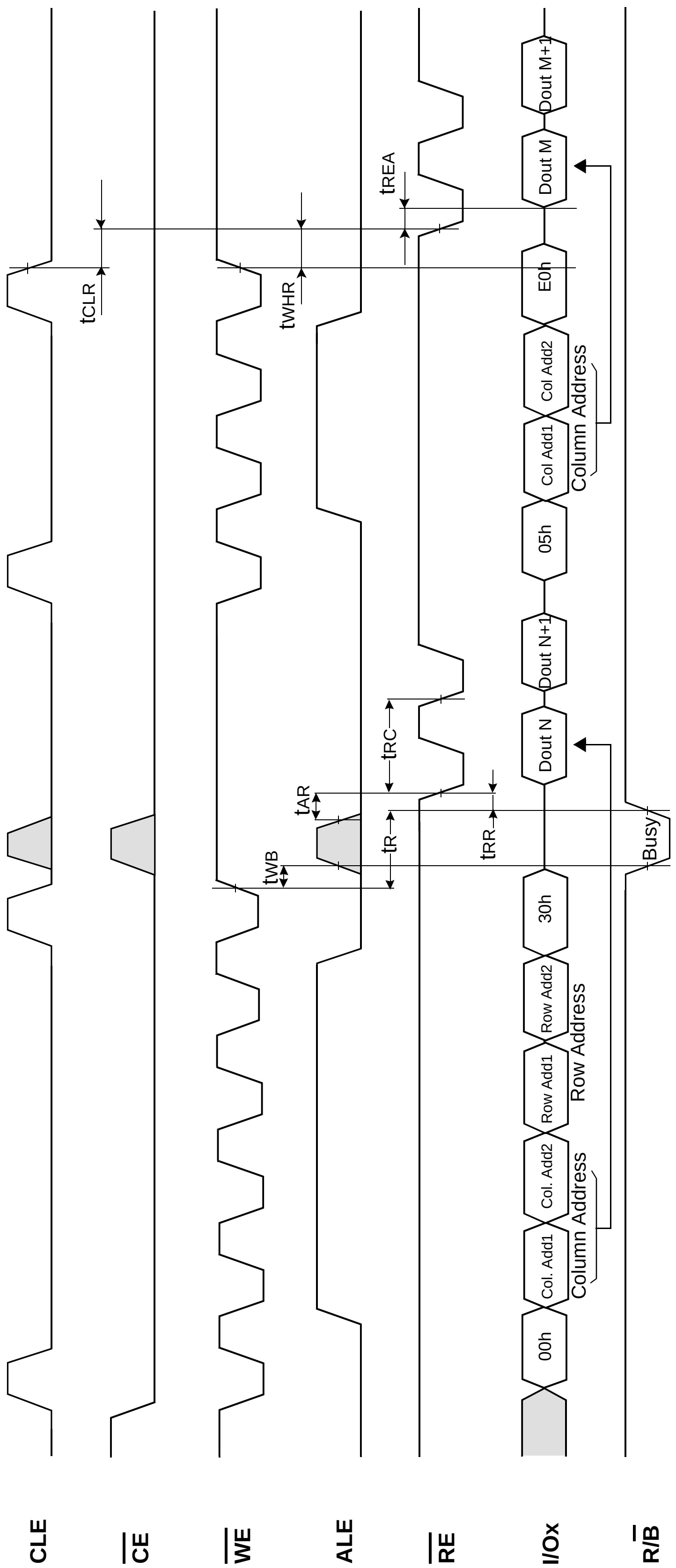
Read Operation



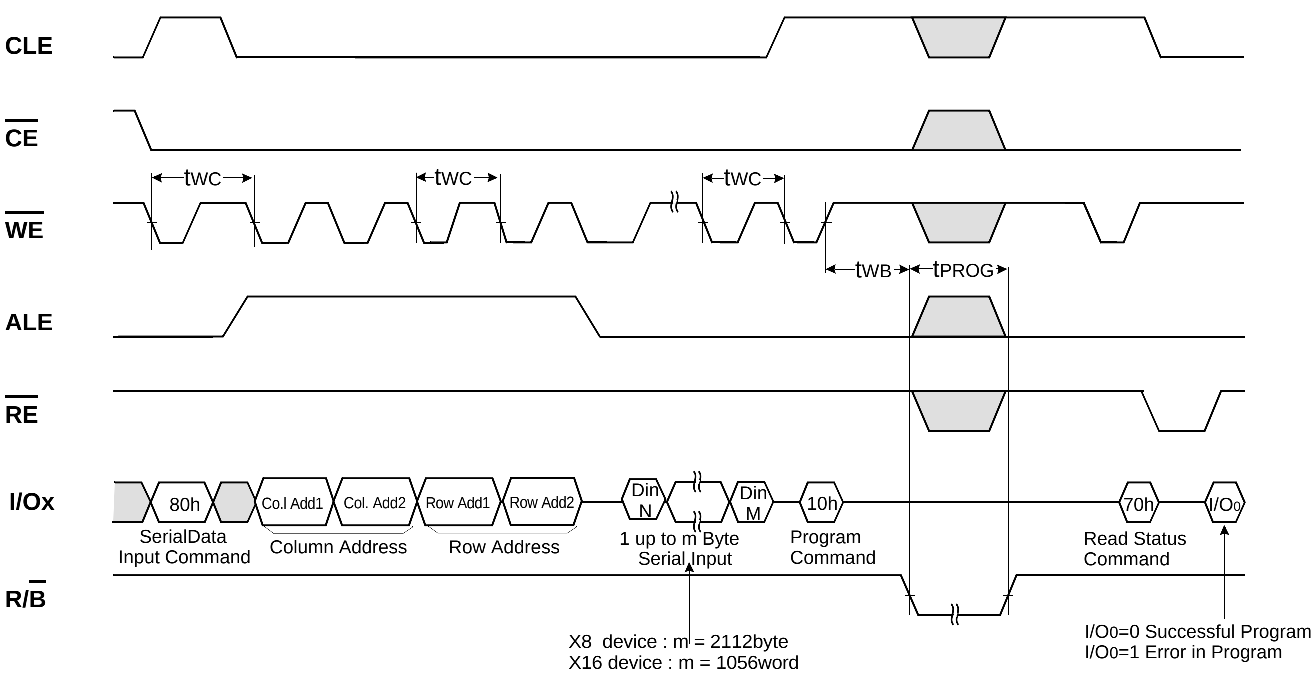
Read Operation(Intercepted by CE)



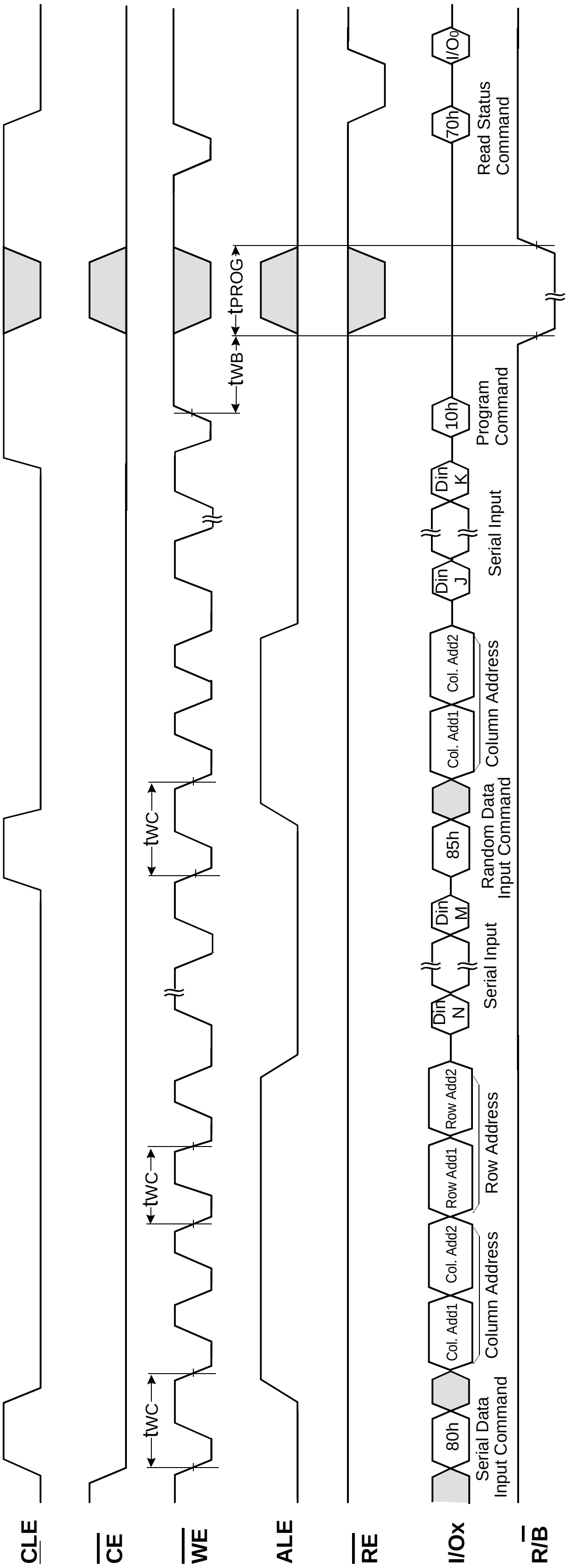
Random Data Output In a Page



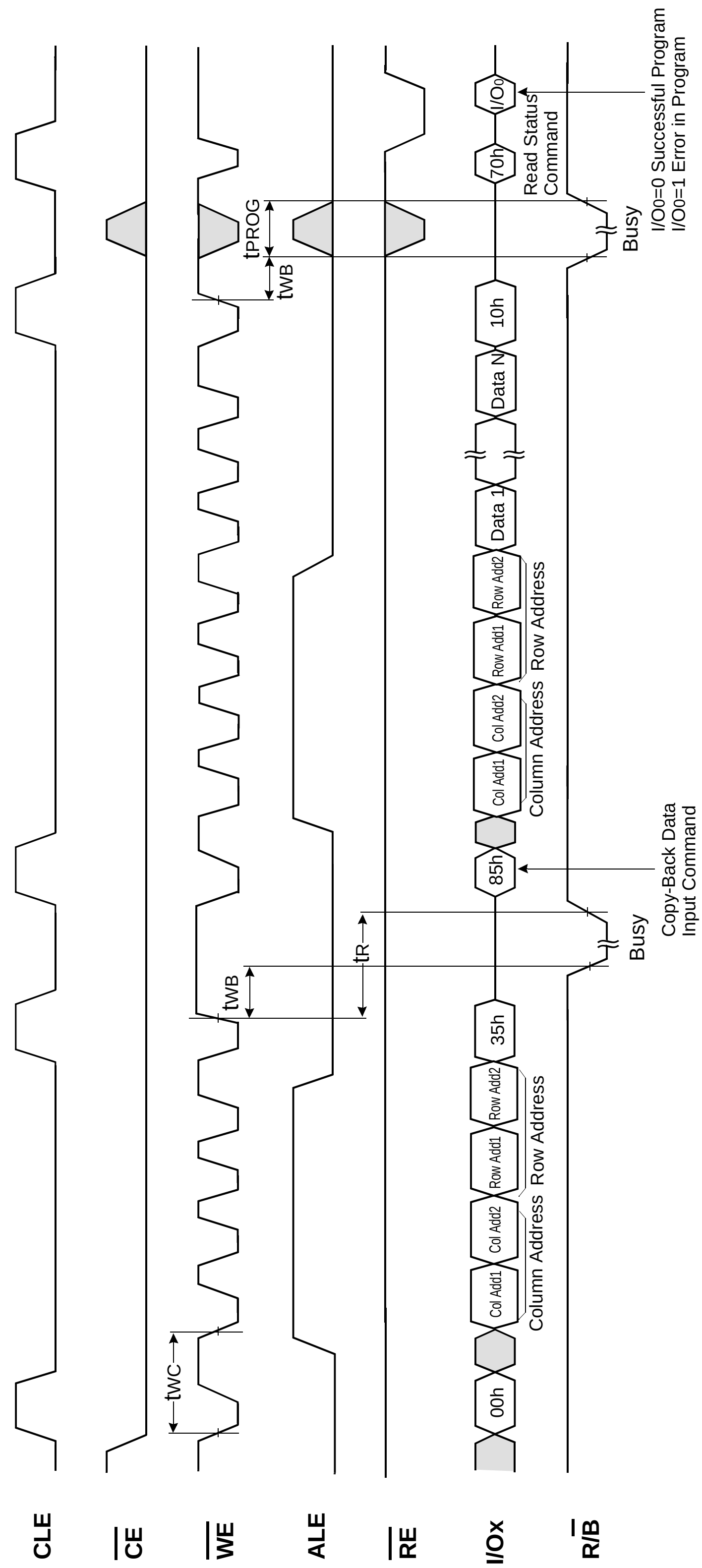
Page Program Operation



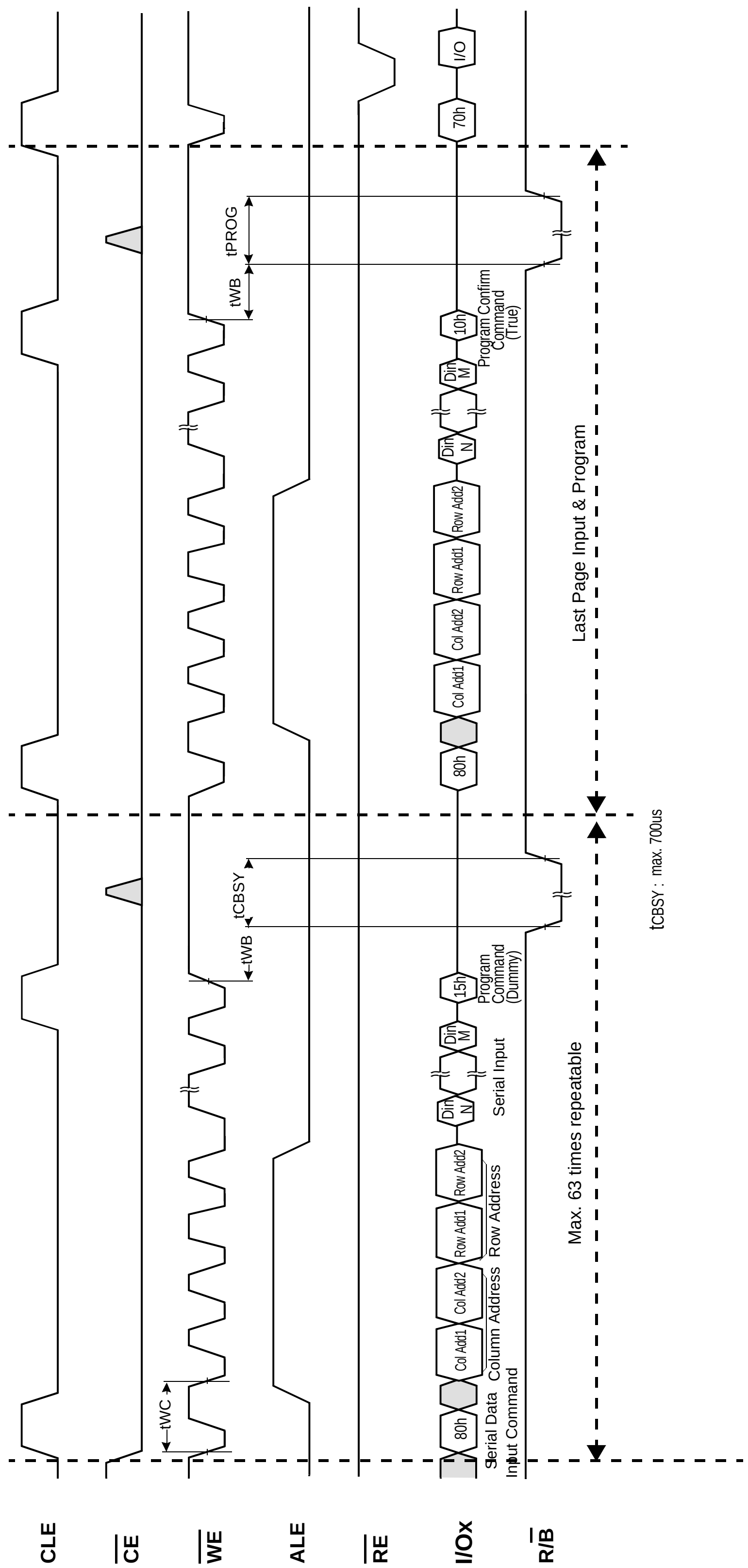
Page Program Operation with Random Data Input



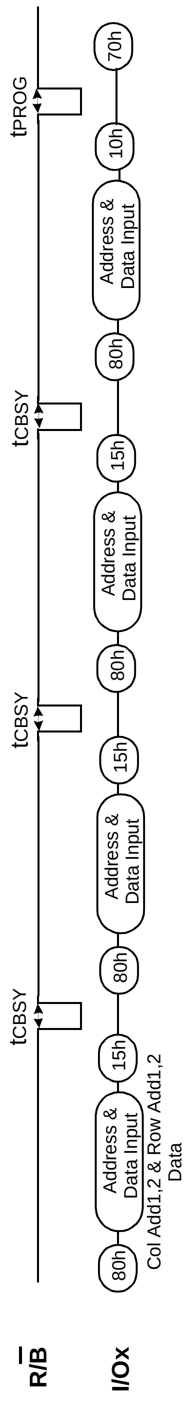
Copy-Back Program Operation with Random Data Input



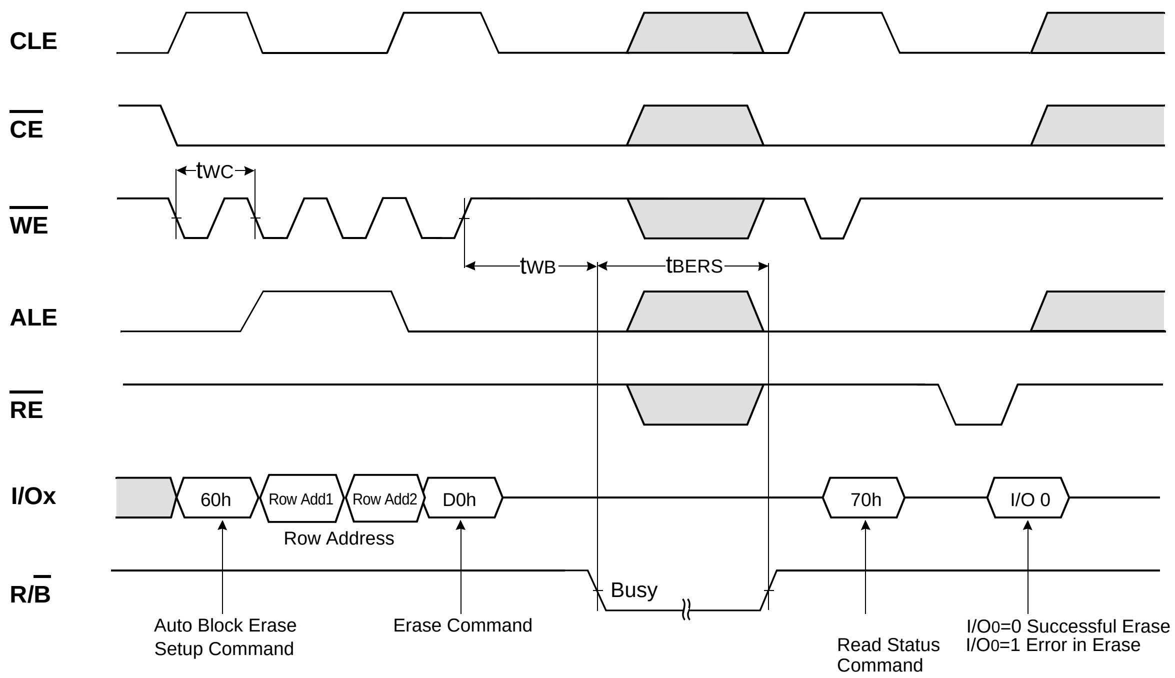
Cache Program Operation(available only within a block)



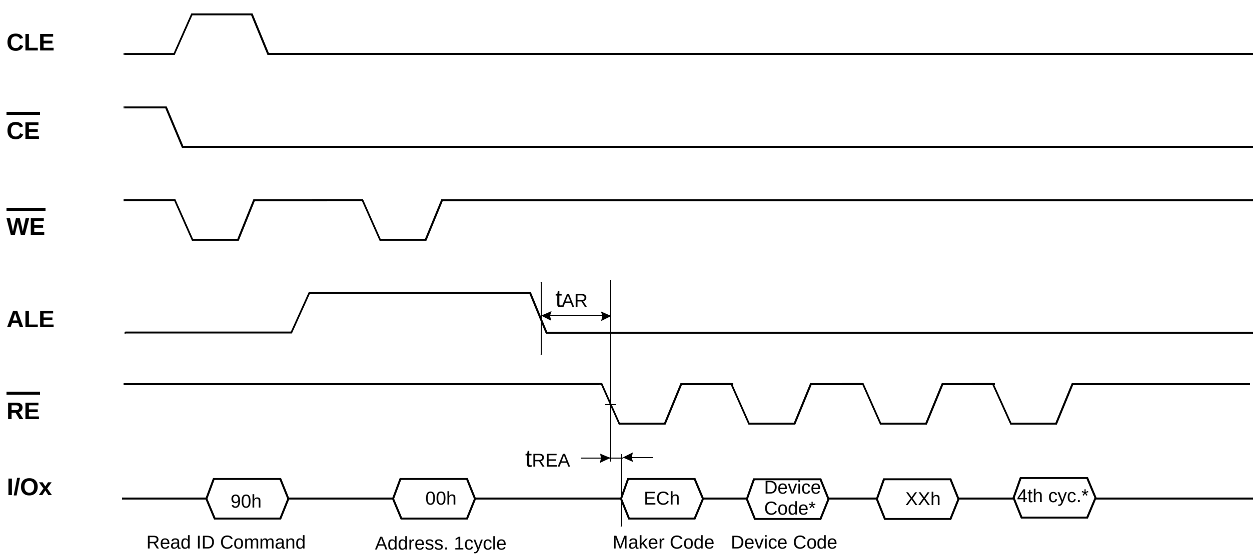
Ex.) Cache Program



BLOCK ERASE OPERATION



Read ID Operation



Device	Device Code*(2nd Cycle)	4th Cycle*
K9F1G08Q0M	A1h	15h
K9F1G08D0M	F1h	15h
K9F1G08U0M	F1h	15h
K9F1G16Q0M	B1h	55h
K9F1G16D0M	C1h	55h
K9F1G16U0M	C1h	55h

ID Defintition Table

90 ID : Access command = 90H

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Don't care
4th Byte	Page Size, Block Size, Spare Size, Organization,Serial access minimum

4th ID Data

ITEM	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	1KB 2KB Reserved Reserved							0 0 1 1	0 1 0 1
Blcok Size (w/o redundant area)	64KB 128KB 256KB Reserved			0 0 1 1	0 1 0 1				
Redundant Area Size (byte/512byte)	8 16						0 1		
Organization	x8 x16		0 1						
Serial Access minimum	50ns 25ns Reserved Reserved	0 1 0 1				0 0 1 1			

Device Operation

PAGE READ

Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing 00h and 30h to the command register along with four address cycles. In two consecutive read operations, the second one doesn't need 00h command, which four address cycles and 30h command initiates that operation.Two types of operations are available : random read, serial page read The random read mode is enabled when the page address is changed. The 2112 bytes(X8 device) or 1056 words(X16 device) of data within the selected page are transferred to the data registers in less than 25µs(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 50ns(1.8V device : 80ns) cycle time by sequentially pulsing RE. The repetitive high to low transitions of the RE clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

Figure 6. Read Operation

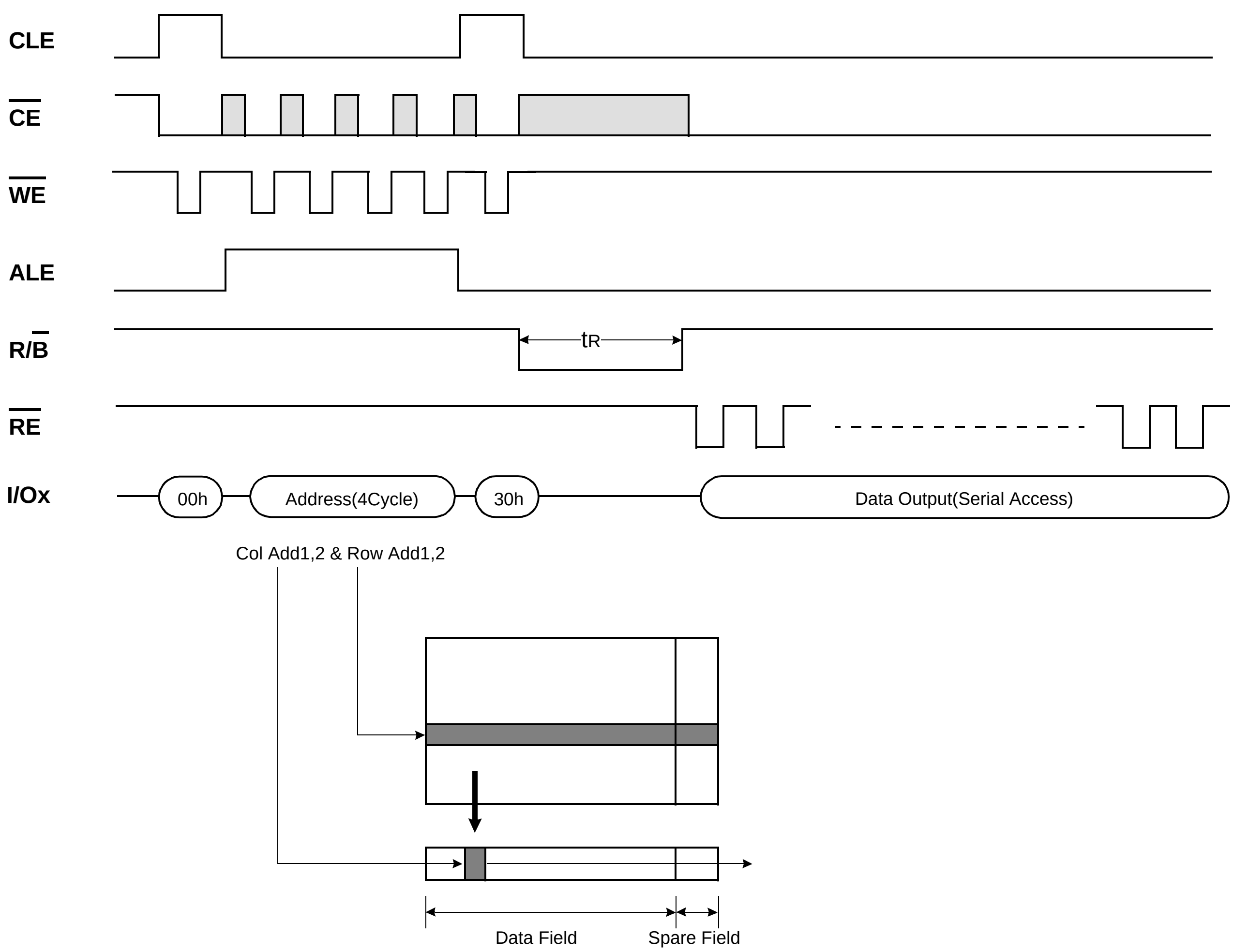
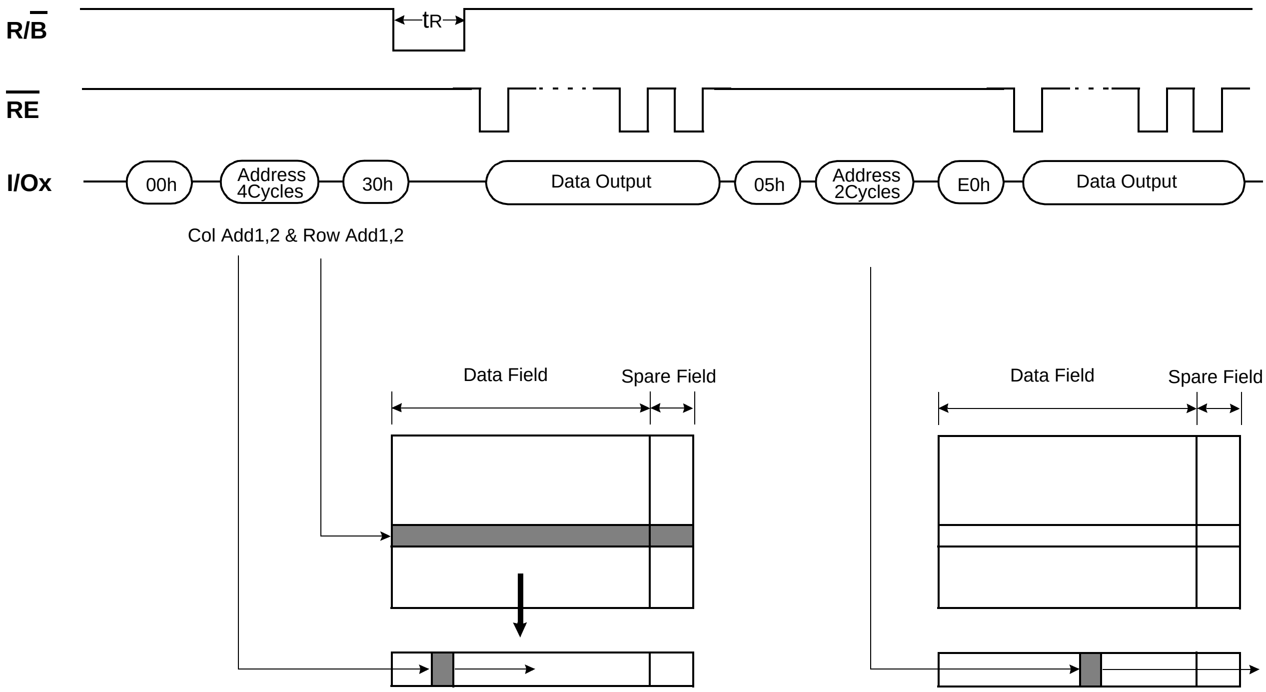


Figure 7. Random Data Output In a Page



PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programing of a word or consecutive bytes up to 2112(X8 device) or words up to 1056(X16 device), in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 4 times for main array(X8 device:1time/512byte, X16 device:1time/256word) and 4 times for spare array(X8 device:1time/16byte ,X16 device:1time/8word). The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 2112bytes(X8 device) or 1056words(X16 device) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.
The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the four cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page.
The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 8). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 8. Program & Read Status Operation

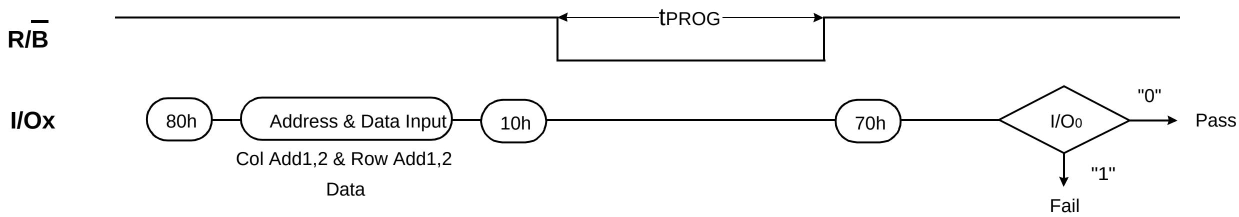
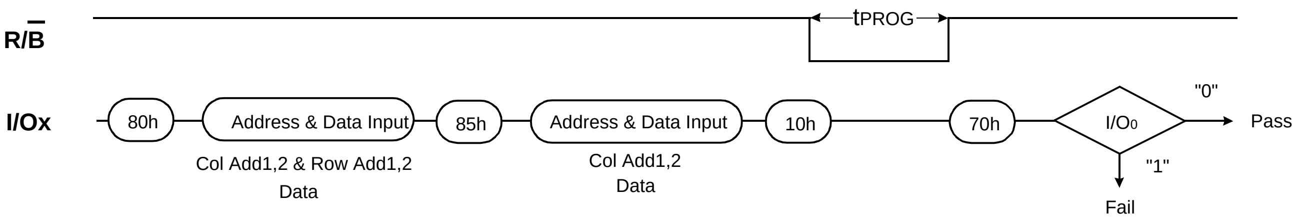


Figure 9. Random Data Input In a Page

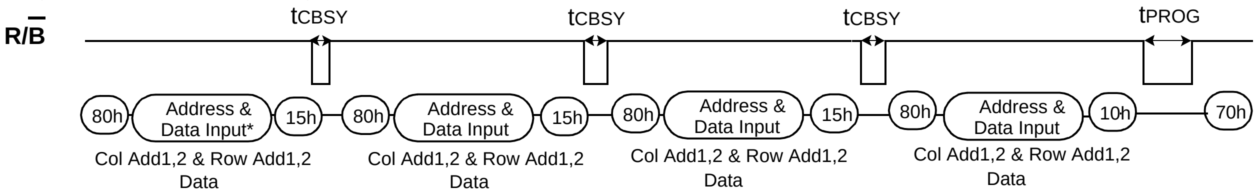


Cache Program

Cache Program is an extension of Page Program, which is executed with 2112byte(X8 device) or 1056word(X16 device) data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data register are programmed into memory cell.

After writing the first set of data up to 2112byte(X8 device) or 1056word(X16 device) into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time(tCBSY) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit(I/O 6). Pass/fail status of only the previouse page is available upon the return to Ready state. When the next set of data is inputted with the Cache Program command, tCBSY is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit(I/O5) for internal Ready/Busy may be polled to identify the completion of internal programming. If the system monitors the progress of programming only with R/B, the last page of the target programming sequence must be progammed with actual Page Program command (10h).

Figure 10. Cache Program(available only within a block)



NOTE : Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

tPROG= Program time for the last page+ Program time for the (last -1)th page
- (Program command cycle time + Last page data loading time)

Copy-Back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112byte(X8 device) or 1056word(X16 device) data into the internal data buffer. As soon as the device returns to Ready state, Page-Copy Data-input command (85h) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 12. **"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But if the soure page has a bit error for charge loss, accumulated copy-back operations could also accumulate bit errors. For this reason, two bit ECC is recommended for copy-back operation."**

Figure 11. Page Copy-Back program Operation

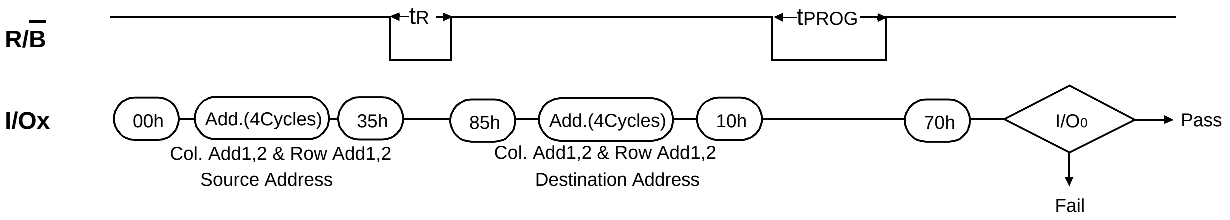
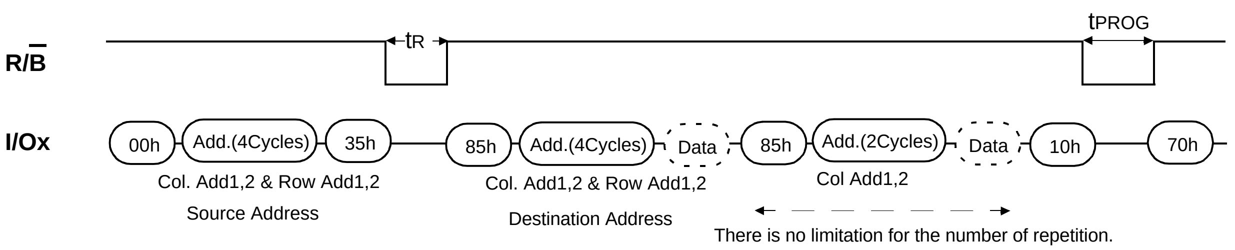


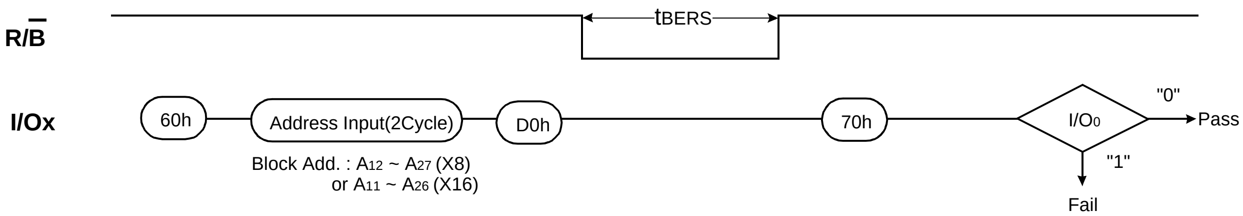
Figure 12. Page Copy-Back program Operation with Random Data Input



BLOCK ERASE

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address A_{18} to A_{27}(X8) or A_{17} to A_{26}(X16) is valid while A_{12} to A_{17}(X8) or A_{11} to A_{16}(X16) is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 13 details the sequence.

Figure 13. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

Table2. Read Staus Register Definition

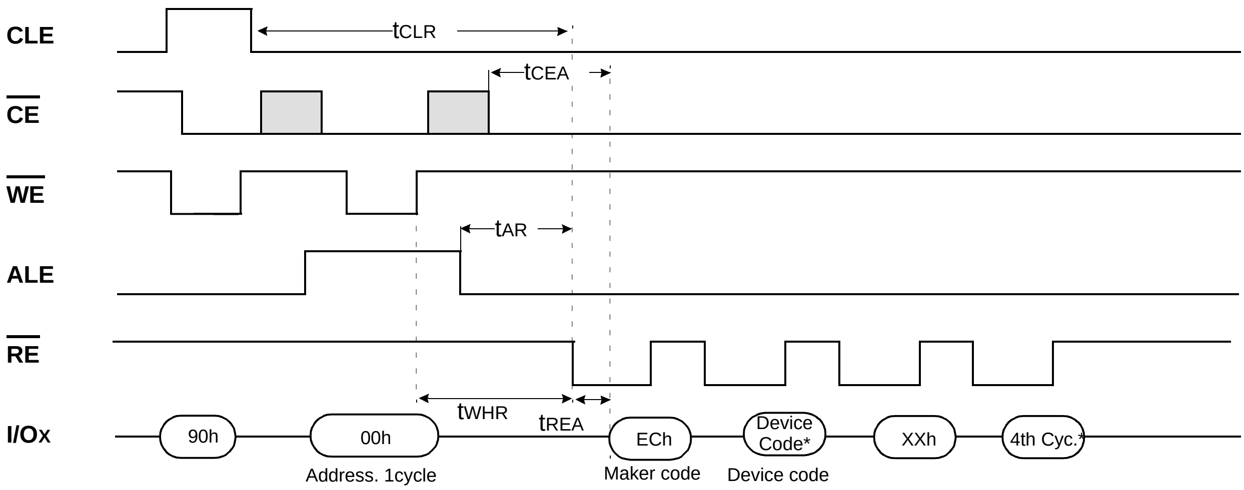
I/O No.	Page Program	Block Erase	Cache Porgram	Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Pass/Fail(N)	Not use	Pass : "0" Fail : "1"
I/O 1	Not use	Not use	Pass/Fail(N-1)	Not use	Pass : "0" Fail : "1"
I/O 2	Not use	Not use	Not use	Not use	"0"
I/O 3	Not Use	Not Use	Not Use	Not Use	"0"
I/O 4	Not Use	Not Use	Not Use	Not Use	"0"
I/O 5	Ready/Busy	Ready/Busy	True Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Protected:"0" Not Protected:"1"
I/O 8~15 (X16 device only)	Not use	Not use	Not use	Not use	Don't -care

NOTE : 1. True Ready/Busy represents internal program operation status which is being executed in cache program mode.
2. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacturer code(ECh), and the device code and XXh, 4th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 14 shows the operation sequence.

Figure 14. Read ID Operation



Device	Device Code*(2nd Cycle)	4th Cycle*
K9F1G08Q0M	A1h	15h
K9F1G08D0M	F1h	15h
K9F1G08U0M	F1h	15h
K9F1G16Q0M	B1h	55h
K9F1G16D0M	C1h	55h
K9F1G16U0M	C1h	55h

RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 3 for device status after reset operation.If the device is already in reset state a new reset command will be accepted by the command register. The R/B pin transitions to low for tRST after the Reset command is written. Refer to Figure 15 below.

Figure 15. RESET Operation

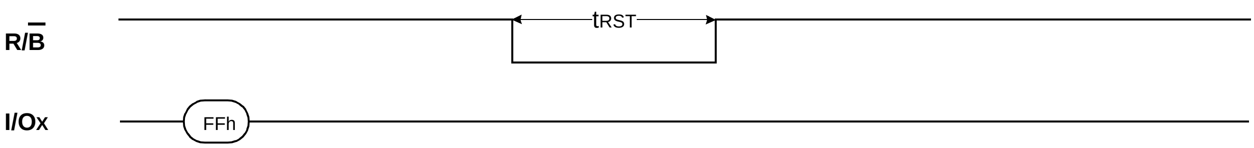


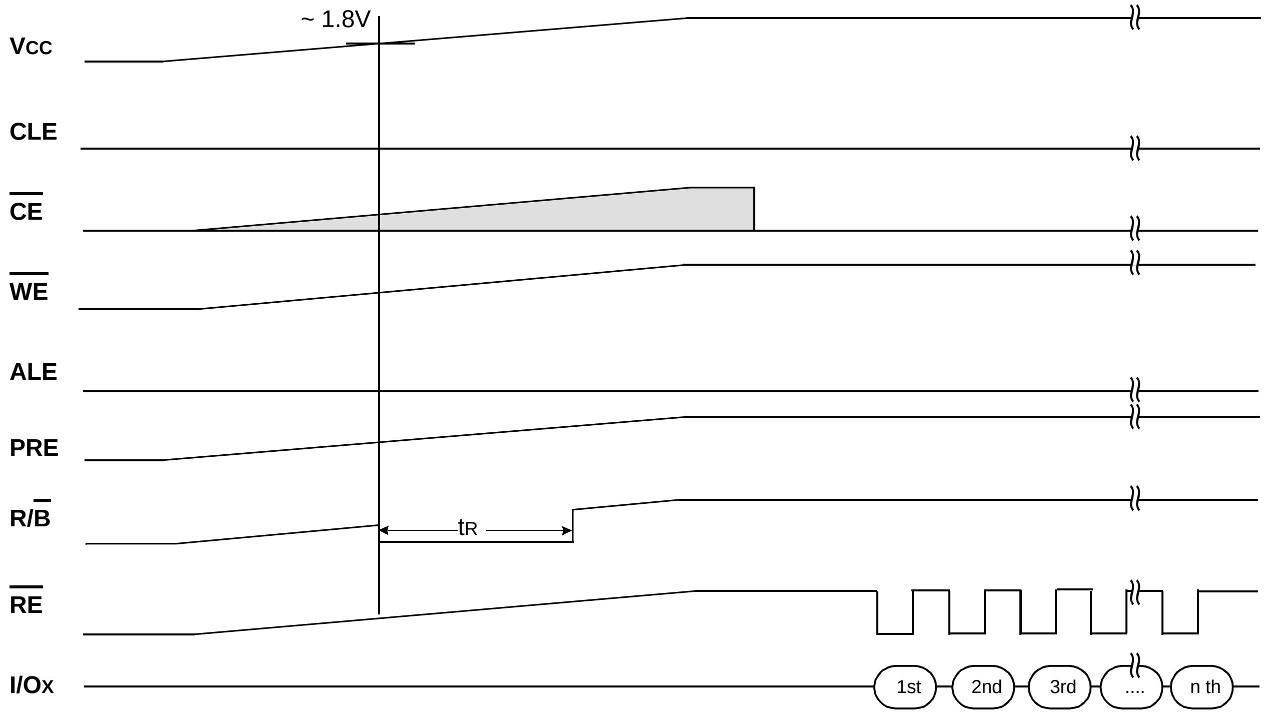
Table3. Device Status

	After Power-up		After Reset
PRE status	High	Low	Waiting for next command
Operation Mode	First page data access is ready	00h command is latched	

Power-On Auto-Read

The device is designed to offer automatic reading of the first page without command and address input sequence during power-on. An internal voltage detector enables auto-page read functions when Vcc reaches about 1.8V. PRE pin controls activation of auto-page read function. Auto-page read function is enabled only when PRE pin is tied to Vcc. Serial access may be done after power-on without latency. Power-On Auto Read mode is available only on 3.3V device(K9F1GXXU0M).

Figure 15. Power-On Auto-Read (3.3V device only)



READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 16). Its value can be determined by the following guidance.

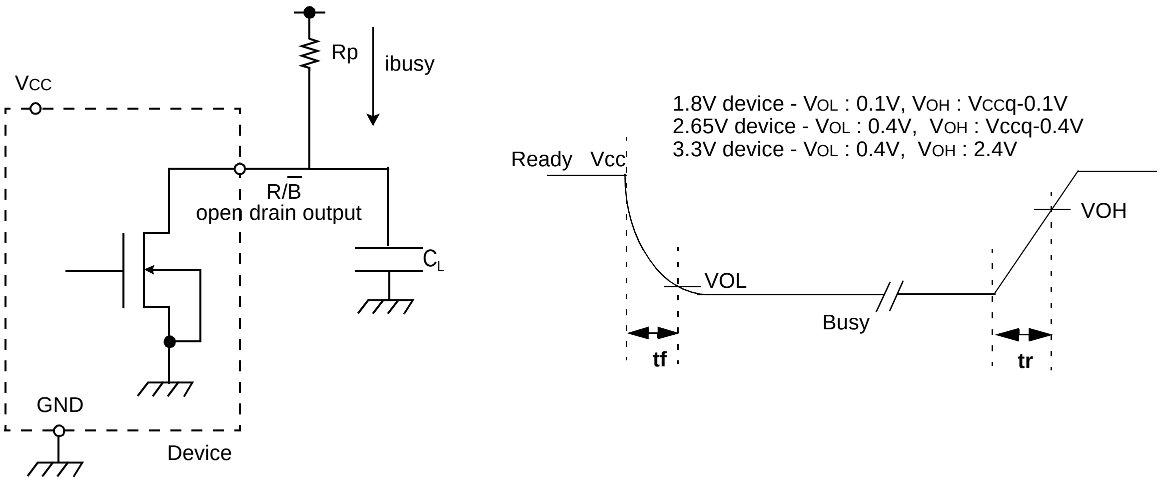
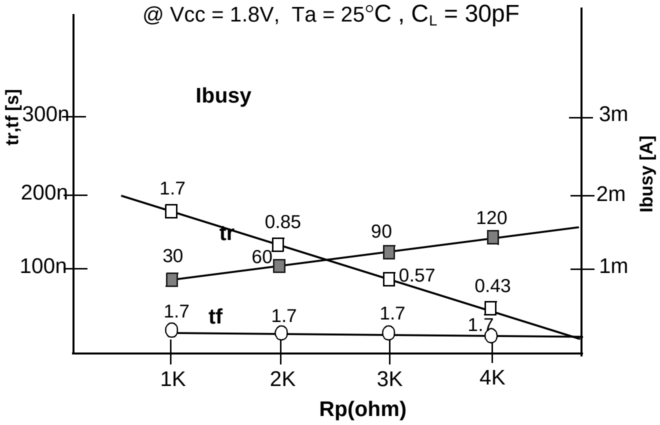
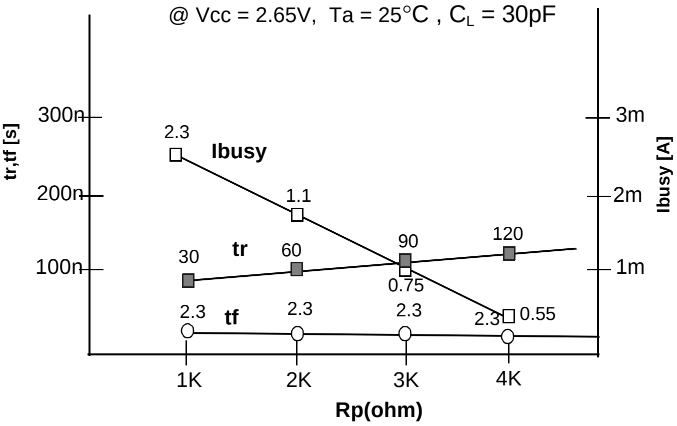
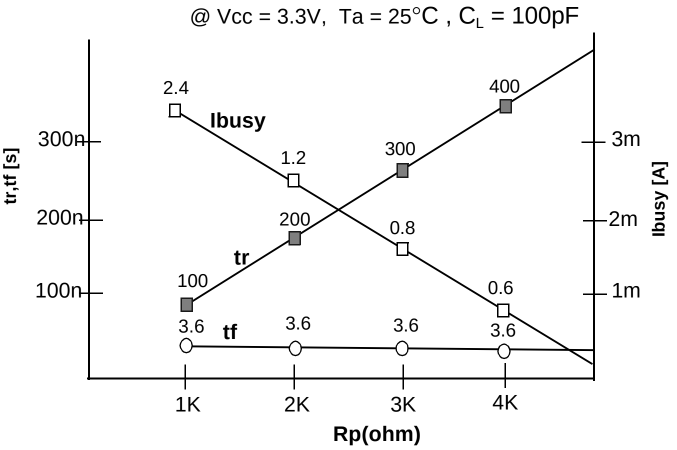


Figure 16. Rp vs tr ,tf & Rp vs ibusy







Rp value guidance

$$Rp(min, 1.8V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

$$Rp(min, 2.65V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{2.5V}{3mA + \Sigma I_L}$$

$$Rp(min, 3.3V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Data Protection & Power up sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.1V(1.8V device), 1.8V(2.65V device), 2V(3.3V device). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10µs is required before internal circuit gets ready for any command sequences as shown in Figure 17. The two step command sequence for program/erase provides additional software protection.

Figure 17. AC Waveforms for Power Transition

